

X1757/MLB

LAST_MODIFICATION= Tue May 5 21:26:43 2020

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	Table of Contents	eli	08/27/2019
2	2	BOM Configuration		06/06/2019
3	3	BOM Configuration		06/06/2019
4	4	PD Parts		06/06/2019
5	5	SOC: Support	ref_soc_h13g	05/04/2020
6	6	SOC: CIO, USB, RESETS, CLOCKS, SWD	ref_soc_h13g	05/04/2020
7	7	SOC: AP I/Os	ref_soc_h13g	05/04/2020
8	8	SOC: LPDP & MIPI	ref_soc_h13g	05/04/2020
9	9	SOC: PCIE	ref_soc_h13g	05/04/2020
10	10	SOC: AOP	ref_soc_h13g	05/04/2020
11	11	SOC: POWER (DDR, SRAM)	ref_soc_h13g	05/04/2020
12	12	SOC: POWER (IO)	ref_soc_h13g	05/04/2020
13	13	SOC: POWER (SOC, CPU, GPU)	ref_soc_h13g	05/04/2020
14	14	SOC: POWER (SRAM)	ref_soc_h13g	05/04/2020
15	15	SOC: POWER (Fixed, PLL's, Filtered)	ref_soc_h13g	05/04/2020
16	16	SOC: GND	ref_soc_h13g	05/04/2020
17	17	SOC: GND-2	ref_soc_h13g	05/04/2020
18	18	SOC: DESENSE CAPS	ref_soc_h13g	10/08/2019
19	19	SPI NOR	ref_soc_h13g	05/04/2020
20	21	SOC: Project Support		
21	50	Secure Element	ref_se_ceres	03/29/2020
22	51	BMU Connector, Btn Logic	tga_140	05/31/2019
23	52	PBUS SUPPLY & BATTERY CHARGER	ref_charger_suona	05/02/2020
24	53	BATTERY CHARGER SUPPORT	ref_charger_suona	05/02/2020
25	57	POWER: 3V8 AON (1/2)	ref_vr_iceman	04/20/2020
26	58	POWER: 3V8 AON (2/2)	ref_vr_iceman	04/20/2020
27	59	POWER: 3V8 AON SUPPORT	T585_REF_VR_ICEMAN_0.30	01/2019
28	77	PMU: SLAVE INPUT PWR & BUCKS	ref_pmu_sera_simetra	04/28/2020
29	78	PMU: SLAVE LDO	ref_pmu_sera_simetra	04/28/2020
30	79	PMU: SLAVE GPIO & GND	ref_pmu_sera_simetra	04/28/2020
31	80	PMU: Slave extra		
32	81	PMU: MASTER INPUT PWR & BUCKS	ref_pmu_sera_simetra	04/28/2020
33	82	PMU: MASTER BUCKS & GND	ref_pmu_sera_simetra	04/28/2020
34	83	PMU: MASTER LDO & GPIO	ref_pmu_sera_simetra	04/28/2020
35	84	PMU: Master extra		
36	121	Power: LDOs	tga_140	05/31/2019
37	122	POWER: 5V, 3V3 Support		
38	123	POWER: 5V S2	ref_vr_5v_lt8642s	04/20/2020
39	127	POWER: 3V3 S2	ref_vr_3v3_tps62135	01/02/2020
40	128	Power: Load Switches	tga_140	05/31/2019
41	130	I2C: SIO, DISP	eli	10/15/2019
42	131	I2C: ISP, AOP	T668	08/01/2019
43	132	I2C: SMC	T668	08/01/2019
44	135	SENSORS: POWER HIGH SIDE (1/2)	t668	08/27/2019
45	136	SENSORS: POWER HIGH SIDE (2/2)	t668	08/27/2019

LAST_MODIFICATION= Tue May 5 21:26:43 2020

PAGE	CSA		SYNC	DATE
46	138	SENSORS: POWER LOW SIDE (1/2)	t668	09/27/2019
47	140	SENSORS: POWER SUPPORT	t668	09/27/2019
48	141	Sensors: Thermal		
49	144	SENSORS: MOTION	t668	09/27/2019
50	149	RIO Connector	tga_140	05/31/2019
51	150	USB-C: High Speed ATC0	ref_usbc_ace2	04/24/2020
52	151	USB-C: High Speed ATC1	ref_usbc_ace2	04/24/2020
53	152	USB-C: Support 1 ATC01	ref_usbc_ace2	04/24/2020
54	153	USB-C: Support 2 ATC01	ref_usbc_ace2	04/24/2020
55	154	USB-C: Port Controller ATC0	ref_usbc_ace2	04/24/2020
56	155	USB-C: Port Controller ATC1	ref_usbc_ace2	04/24/2020
57	156	USB-C: Connector(s)	ref_usbc_ace2	09/26/2019
58	157	USB-C: HS Level Shifters	ref_usbc_ace2	04/24/2020
59	159	USB-C: Project Specific		
60	200	WIFI/BT: MODULE	ref_wireless_rasputin	04/28/2020
61	201	WIFI/BT: ANTENNA and GND	ref_wireless_rasputin	04/28/2020
62	220	STORAGE: SSD0 S5E <0>	ref_storage_s5e	05/02/2020
63	221	STORAGE: SSD0 S5E <1>	ref_storage_s5e	05/02/2020
64	224	STORAGE: NON OCARINA SUPPORT	ref_storage_non_ocarina_support	02/17/2020
65	230	STORAGE: SSD Support	T668	08/01/2019
66	231	SECDIS: MIPI MUX	ref_secdis_mipimux	10/07/2019
67	236	eDP Display Connector	tga_140	05/31/2019
68	237	DISPLAY POWER SEQUENCER	ref_panelpwr_bnj	05/02/2020
69	238	BEN: CONTROLLER	ref_blc_ben	11/20/2019
70	239	BEN: KEYBOARD	ref_blc_ben	11/20/2019
71	242	SECDIS: AMR	ref_secdis_amr	10/21/2019
72	243	SECDIS: FPGA	ref_secdis_sak	04/28/2020
73	244	Audio Level Shifters	ref_spkramp_tas5770	11/18/2019
74	246	AUDIO AMPLIFIERS (1/2)	ref_spkramp_tas5770	04/20/2020
75	248	Audio Connectors	tga_140	05/31/2019
76	253	Trackpad Support	ref_ipd_oregano	08/01/2019
77	254	IPD Combined Connector	card_ipd_oregano	08/01/2019
78	260	Power Aliases - 1	tga_140	05/31/2019
79	261	Power Aliases - 2	tga_140	05/31/2019
80	263	Signal Aliases 1		
81	264	Signal Aliases 2		
82	270	DEBUG	tga_140	05/31/2019
83	281	Desense		
84	500	17.2 RULES	eli	10/15/2019
85	501	17.2 PHYSICAL CSETS	eli	10/15/2019
86	502	17.2 SPACING CSETS, ISO	eli	10/15/2019
87	503	17.2 SPACING CSETS, CLASS-CLASS	eli	10/15/2019
88	601	BOM OPTION TABLES	t668	11/01/2019
89	602	BOM GROUPS	t668	11/01/2019
90	610	BOM Alternates		

A Module Parts

TBT Burnside Bridge

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S90561	2	IC,TBT,BBR,SLM77,PRQ,A1,ROA105	UF000,UF100	CRITICAL	TBT_BB:PRQA1

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S92158	2	IC,C93217,ACE2,B2,USB,PWR,SM,W/HW,BGA123	UF400,UF500	CRITICAL	ACE2:B2_BGA

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20641	2	IC,PWRROT,C932234,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6
338S90628	2	IC,PWRROT,C932236,B0,LSB1,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_LSB1_OTP6

Secure Element

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19915	1	IC,SEC238V,B1,C0RES,DEV,RY,SW/HV,MALCSPR1	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SEC238V,B1,C0RES,DEV,SW/H3,MALCSPR1	U5000	CRITICAL	SE:DEV_SW_H3
338S90630	1	IC,SEC238V,B1,C0RES,PROD,VER/H4,MALCSPR1	U5000	CRITICAL	SE:PROD_SW_MU

B Programmable Parts

TBT ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S90133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,U50N8	UF260	CRITICAL	TBT_ROM:BLANK
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S90232		335S90133	TBT_ROM:BLANK	UF260	rdar://problem/59598337
341S91617	1	ROM,TBT/ACE (V31.5) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP0
341S91676	1	ROM,TBT/ACE (V2.45.0.7) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP1

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20613	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,X50N8	U1970	CRITICAL	SOC_ROM:BLANK_ORIG
335S90494	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,4X3,S0N8	U1970	CRITICAL	SOC_ROM:BLANK
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S90500		335S90494	SOC_ROM:BLANK	U1970	rdar://problem/59964804

Vinafix.com

A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,ALTERNATE,COMMON,CNN_IC,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_WIRELESS,MLB_MECH,MLB_MISC,MLB_BLC,EVT,SECDIS_EXT_CLK,DMIC_CLK_100MH
MLB_USBC	TBT_BB:PRQA1,ACE2:B2_BGA,UPC_ATCRTMR_INT,UPC_EUSBLS_INT,EUSB_LS:B0_LSB1_OTP6
MLB_PROGPARTS	WFBT_ROM:BLANK,SOC_ROM:BLANK,TBT_ROM:PP1,SE:PROD_SW_MU
MLB_POWER	PBUS_3S,MPMU_IC:B0,SPMU_IC:A1,P3V8AON_IC:A1_R0B0
MLB_WIRELESS	WLBT:ES6_3_M
MLB_MECH	SHLD_CAN_BSB:EVT,SHLD_CAN_ICE:EVT
MLB_MISC	BOARD_ID,SYSDET:FET,BOOT_CONFIG2,LOADISNS
MLB_DEV	DEVELOPMENT,WLBT_DBG,USBC_DBG
MLB_BLC	BLC_BEN_IC:V7,BLC_LEDS_PER_STRING:16,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KB0_BOOST_USED:YES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00339	1	COMMON PARTS,MLB,X1757	CBOM	CRITICAL	CNN_PARTS_BOM
685-00377	1	PARTS,SSDAND1,MLB,X1757	P1BOM	CRITICAL	PARTS_SSDAND1
985-01176	1	DEV PARTS,MLB,X1757	DEV1	CRITICAL	DEV_PARTS_BOM
051-05392	1	SCHEM,MLB,X1757	SCHEM	CRITICAL	SCHEM
820-02016	1	PCBF,MLB,X1757	PCBF	CRITICAL	PCBF

B Build Specific Groups

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID1,BOARDID2
PROT00	BOARD_REV3,BOARD_REV2,BOARD_REV1,BOARD_REV0
PROT01	BOARD_REV3,BOARD_REV2,BOARD_REV1
EVT	BOARD_REV3,BOARD_REV2,BOARD_REV0

Pull-ups: 0x0000110

Pull-downs: 0x0000

Pull-downs: 0x0001

Pull-downs: 0x0002

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,DCDC_USBC,MLB_POWER,MLB_MECH,MLB_MISC,MLB_BLC,EVT
DCDC_USBC	UPC_ATCRTMR_INT,UPC_EUSBLS_INT

D Reference Design Pack Options

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPT_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
NO_DFR
FTCAM
HAS_LID

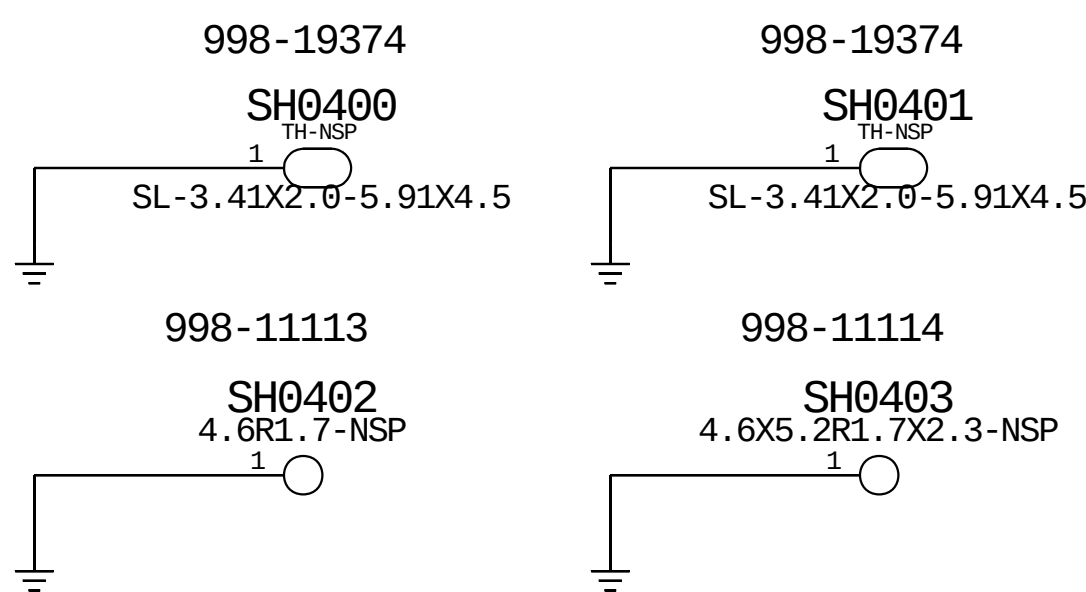
PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS-D12
3V3_S2_PBUS-D2
3V8_AON_PBUS-B12
3V8_AON_I2C-DEV
NO_AMR_INTERPOSER_LEFT
NO_AMR_INTERPOSER_RIGHT
PKGS:SMALL_PITCH
ACE2_SS_CAP

PACK_OPTIONS TO INCLUDE IN NETLIST
PROD_SECDIS
JTAG_SECDIS:NO
PROTO_PULLDOWN_SECDIS
80UM_STEN
INTERNAL_DISPLAY
CHGR_40W

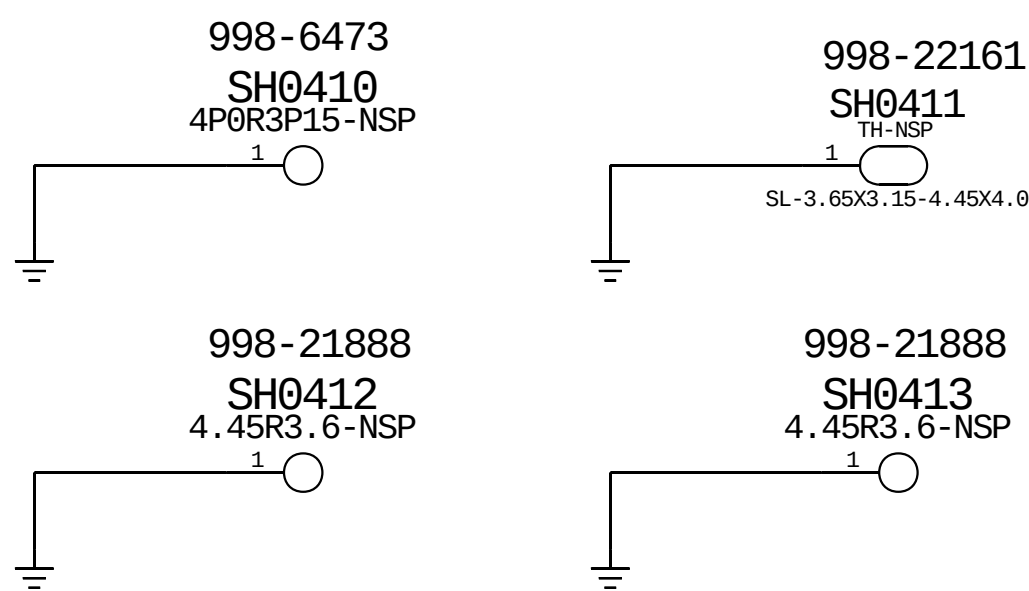
PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_DBG_CONN
SPKRAMP_A
PORTABLE
SMALL_NOR
SPKRAMP_LVL_SON

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_TP
CHGR_TP_BOT
3V8_EXT_DIODE

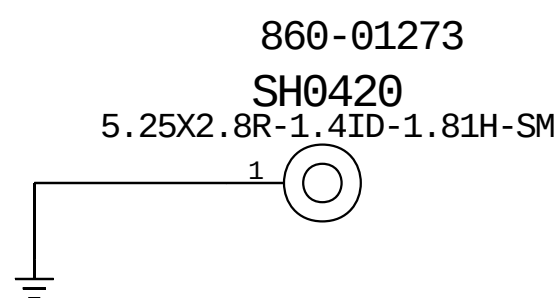
A Mounting Holes



B Heatsink Mounting Holes



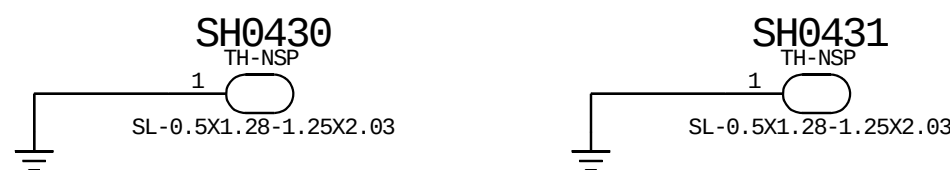
C Antenna Cowling Bosses



D Burnside Bridge Shield Can

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-19070	1	SHIELD CAN, BURNSIDE BRIDGE, X1419	SHLD1	CRITICAL	SHLD_CAN_BSB
806-26240	1	SHIELD CAN, BURNSIDE BRIDGE, X1739	SHLD1	CRITICAL	SHLD_CAN_BSB:EVT

Plated slots for shield can



E Sled, Thermal Module

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-25230	2	SLED, SOLDER, X1757	SLD1, SLD2	CRITICAL	

F Inductor Shield Fence

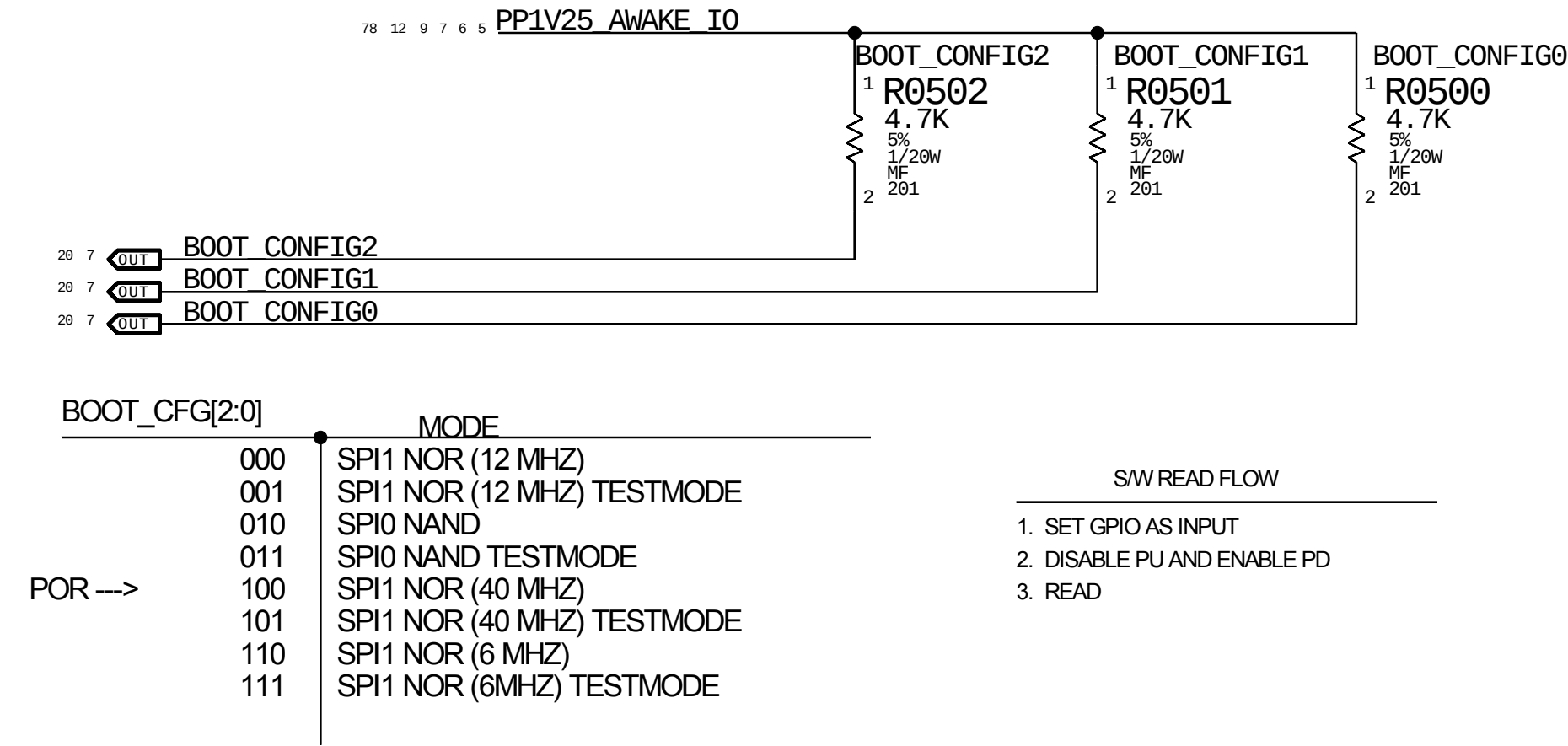
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-27192	1	SHIELD FENCE, ICEMAN, INDUCTORS, X1739	SHLD2	CRITICAL	SHLD_CAN_ICE
806-27475	1	SHIELD FENCE, INDUCTORS, X1739	SHLD2	CRITICAL	SHLD_CAN_ICE:EVT

Plated slots for shield can

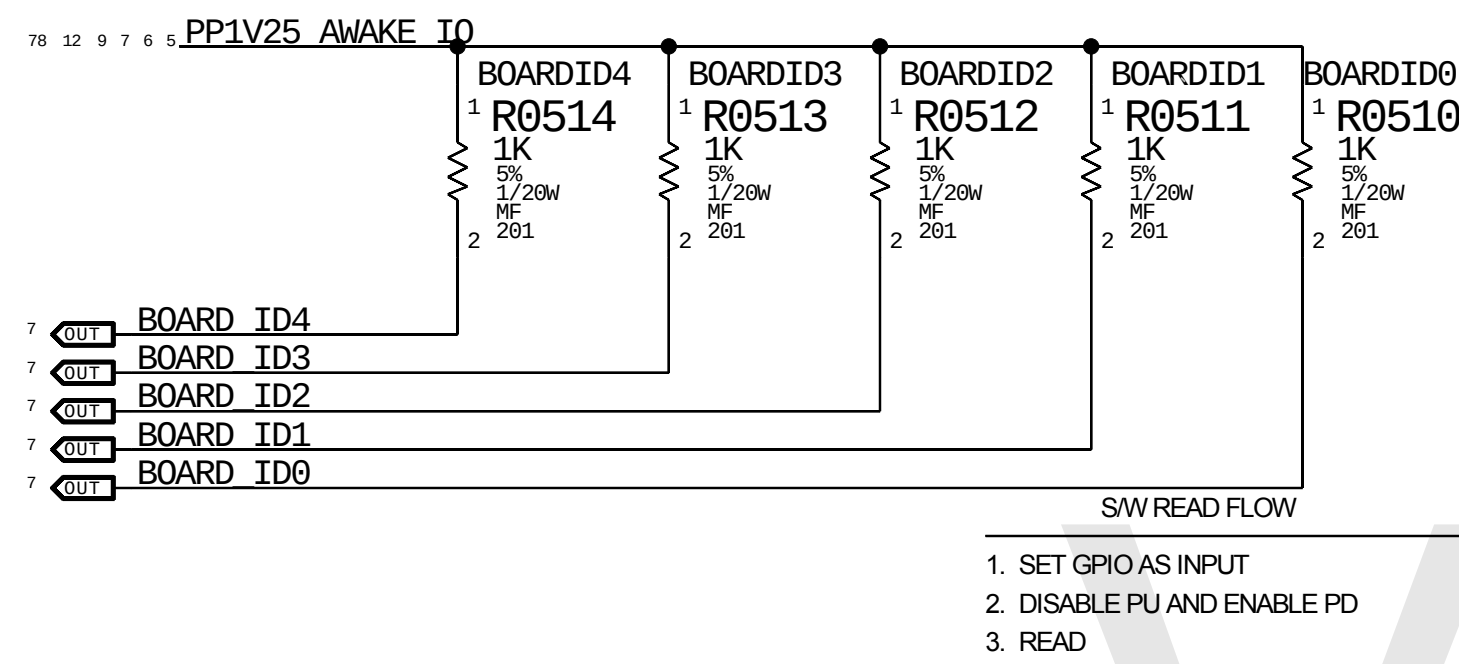


OK2INTEGRATE

BOOT CONFIG ID

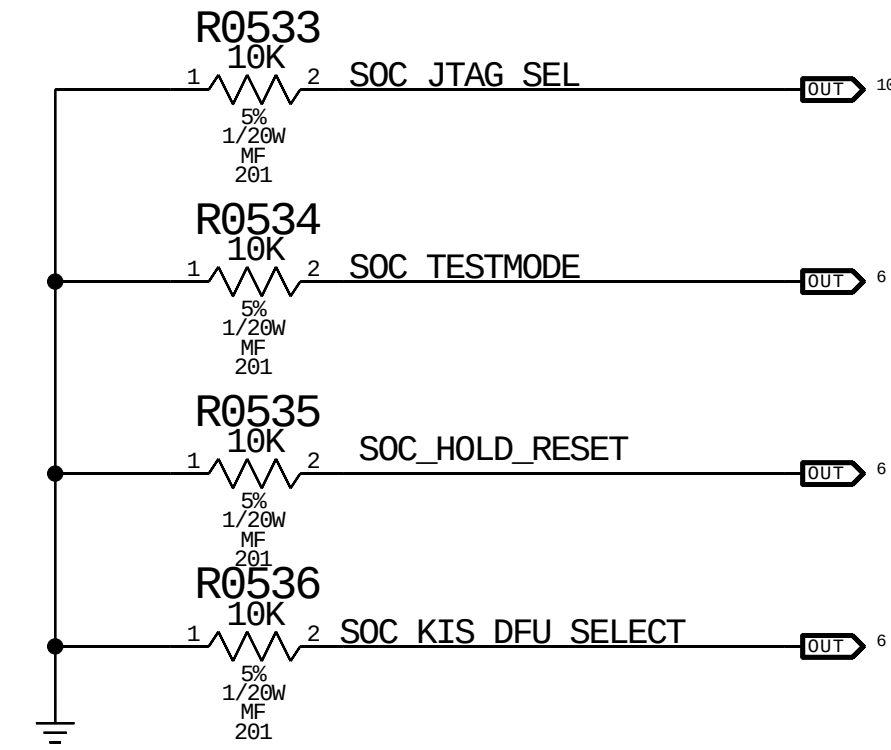
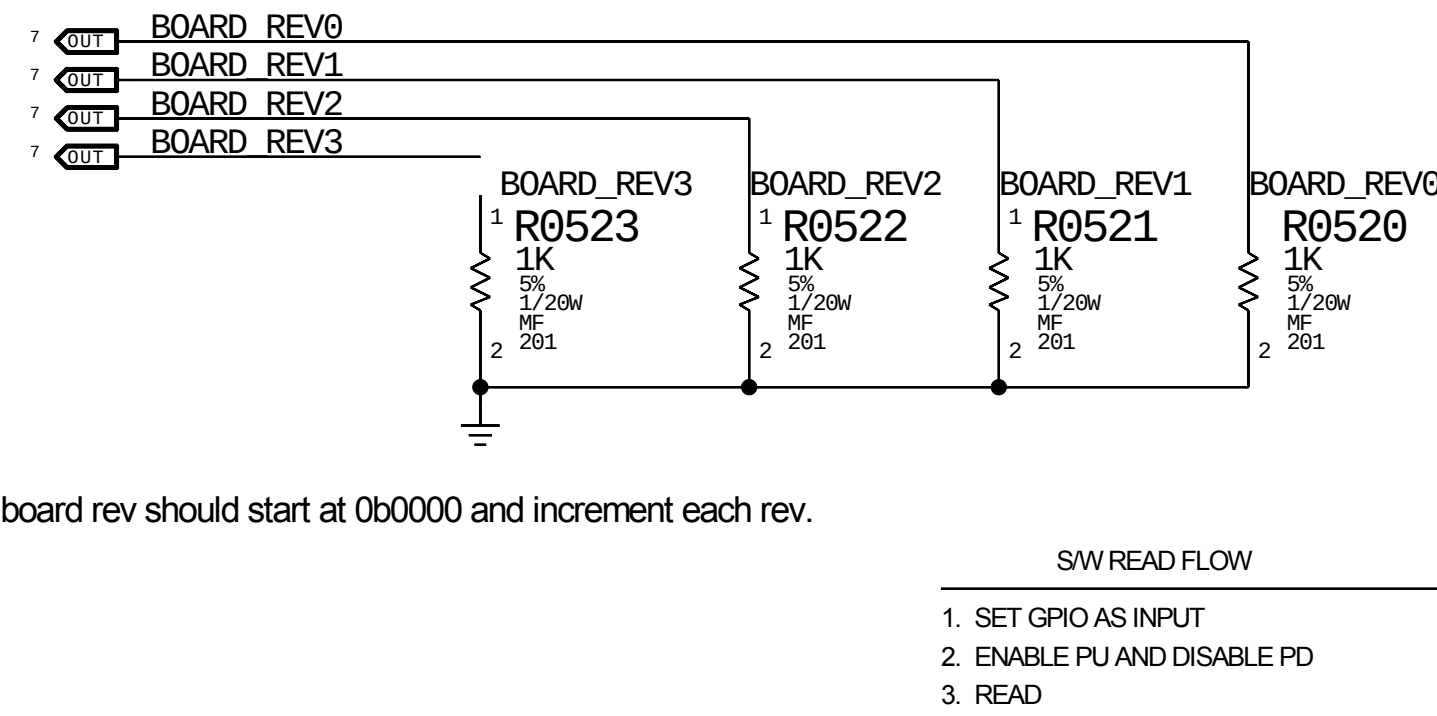


BOARD ID

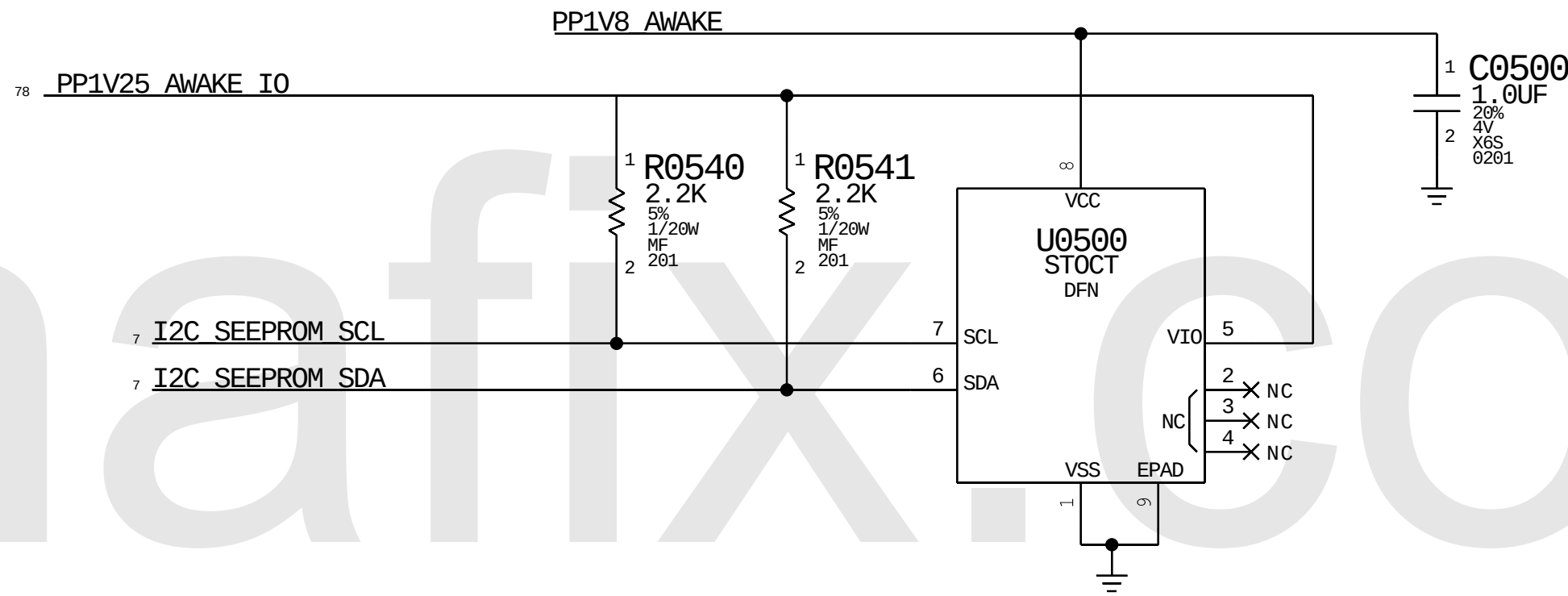


BOARD REVISION

NOTE: STUFFING RESISTOR MEANS 0



SEP EEPROM (128-Kbit)
(Write: 0xA2, Read 0xA3)
APN:335S00455



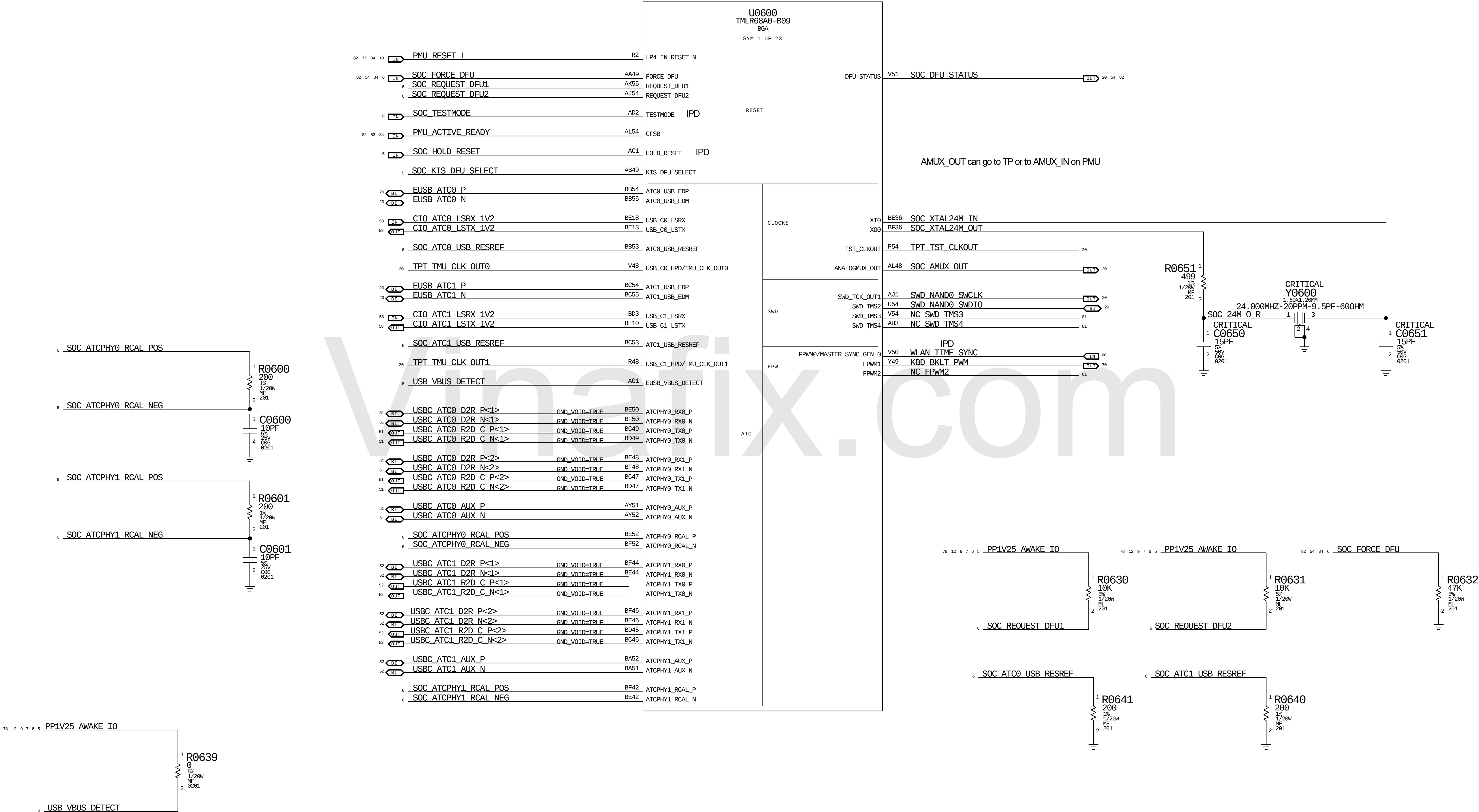
PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	720 DELAY CSV FILE NAME
U0600	TGA_PINDELAY_2020_03_26.csv

OCELOT I2C pulls

OK2INTEGRATE

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM

OMIT_TABLE

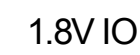


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON, 24MHZ, XTAL
197S0588	197S0591		Y0600	TXC, 24MHZ, XTAL

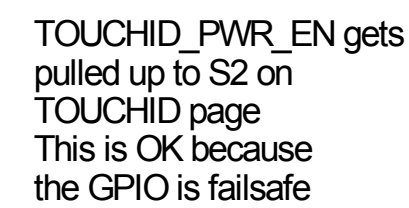
BOM_COST_GROUP=SOC

SOC: CIO, USB, RESETS, CLOCKS, SWD

all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP



PORTABLES SHOULD NC TRIGGER2

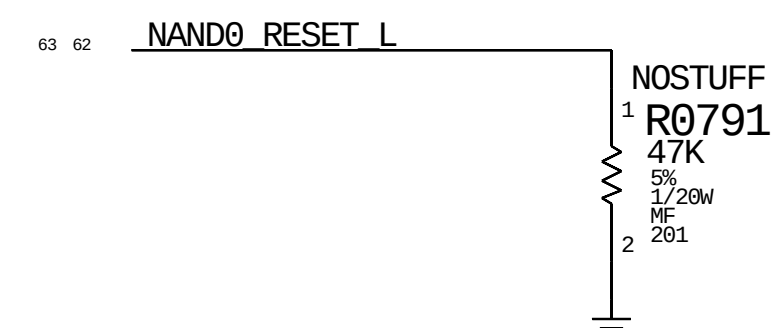


1.8V IO

Use UART2 if your wireless module is 1.2V IO

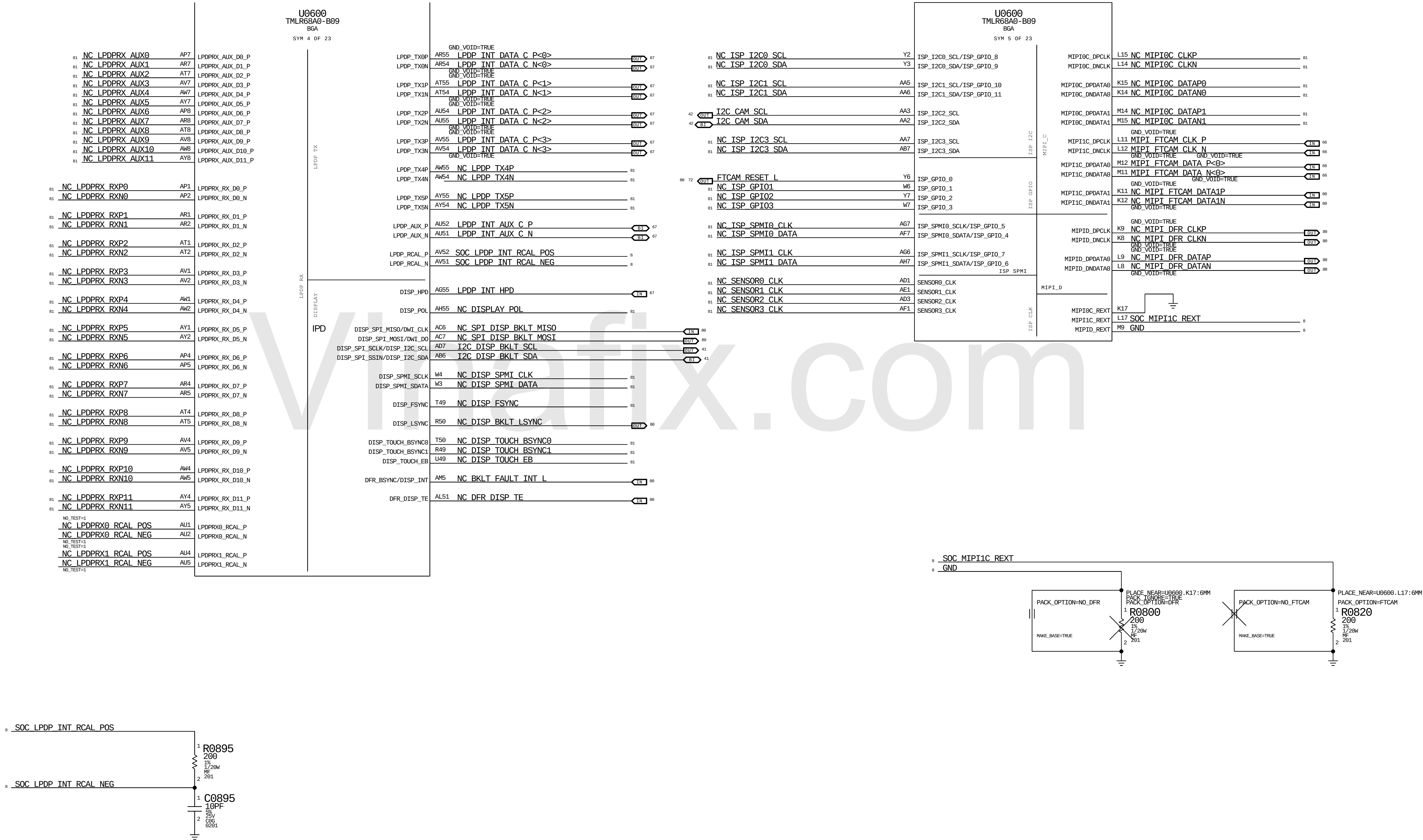
1.8V IO

R2D is for desktop only



SOC: AP I/Os	
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SOC: LPDP & MIPI

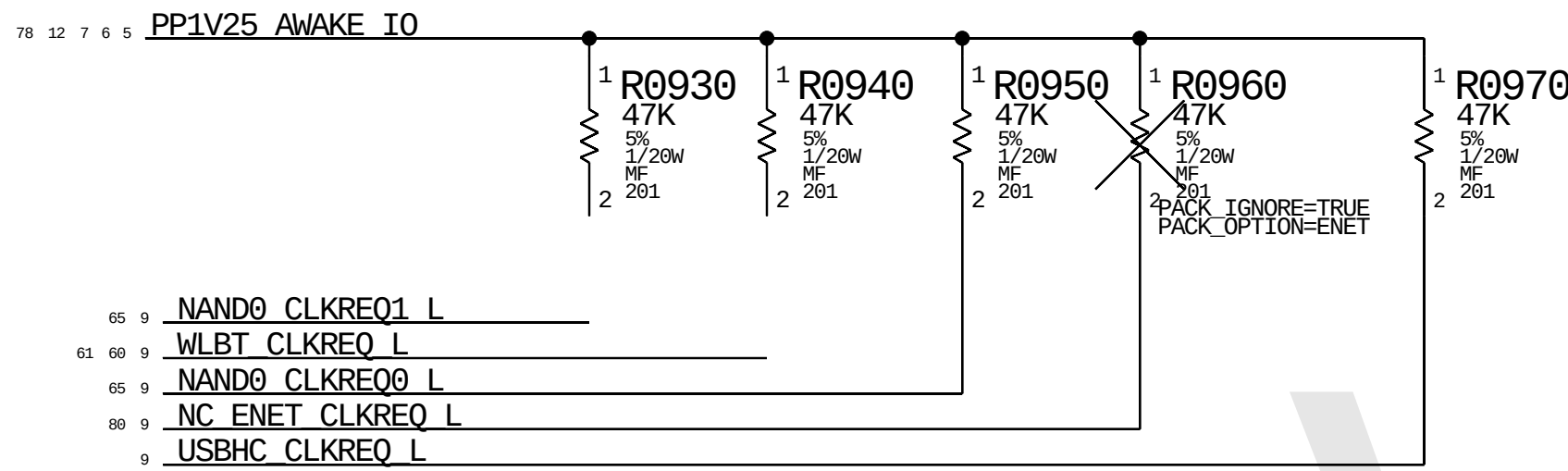


OK2INTEGRATE

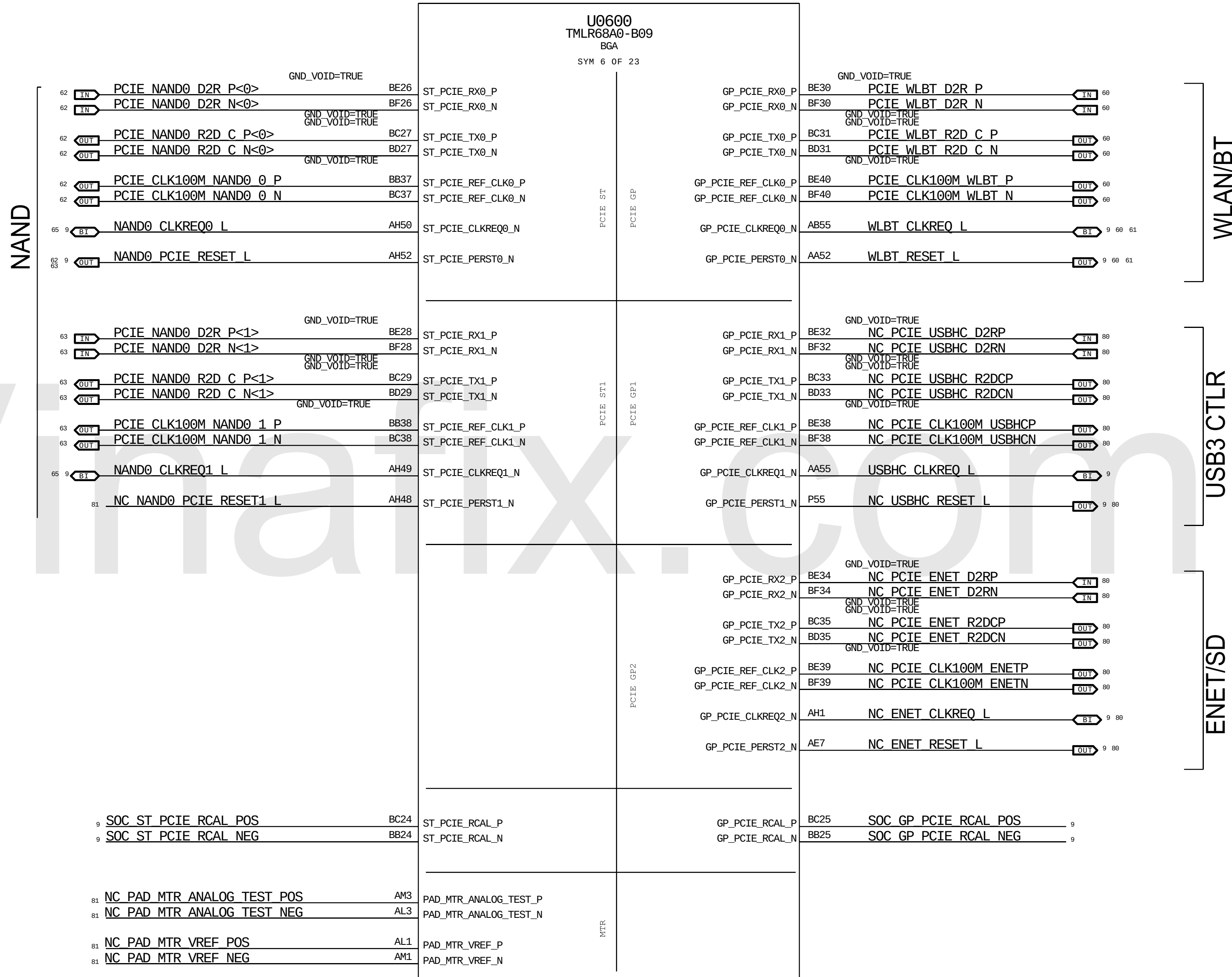
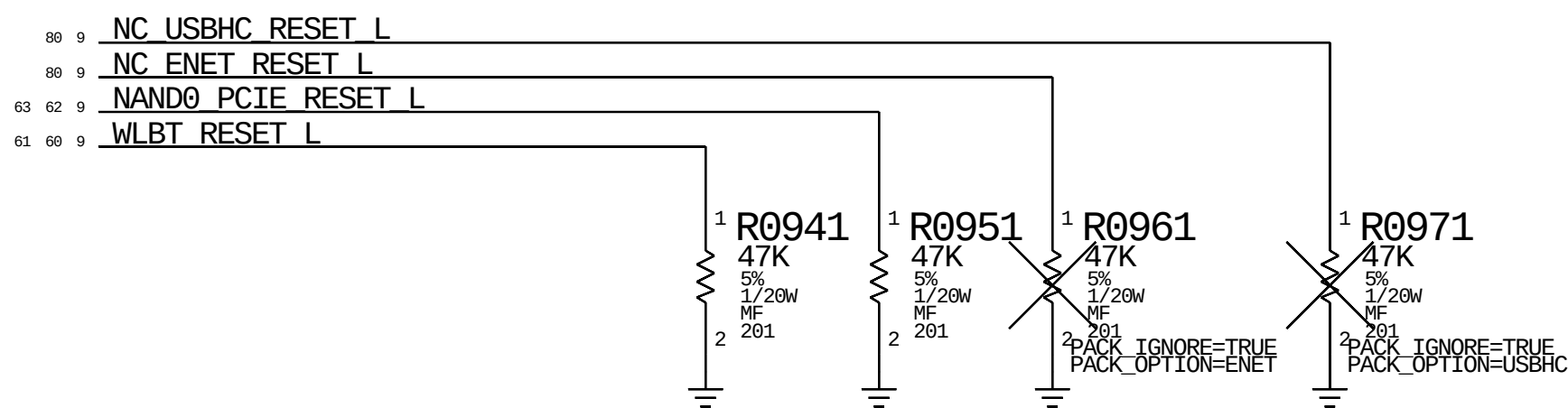
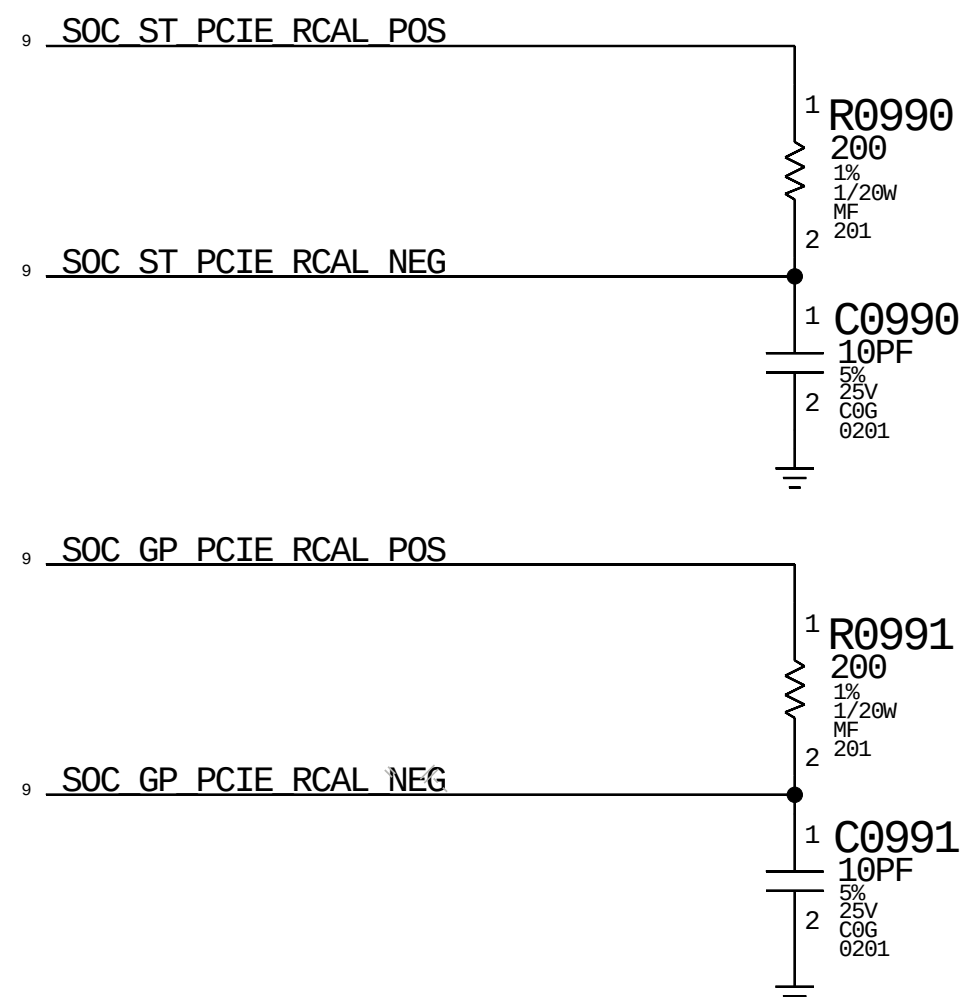
SOC: PCIE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

R0970 IS NEEDED DUE TO RDAR://53793006



TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?



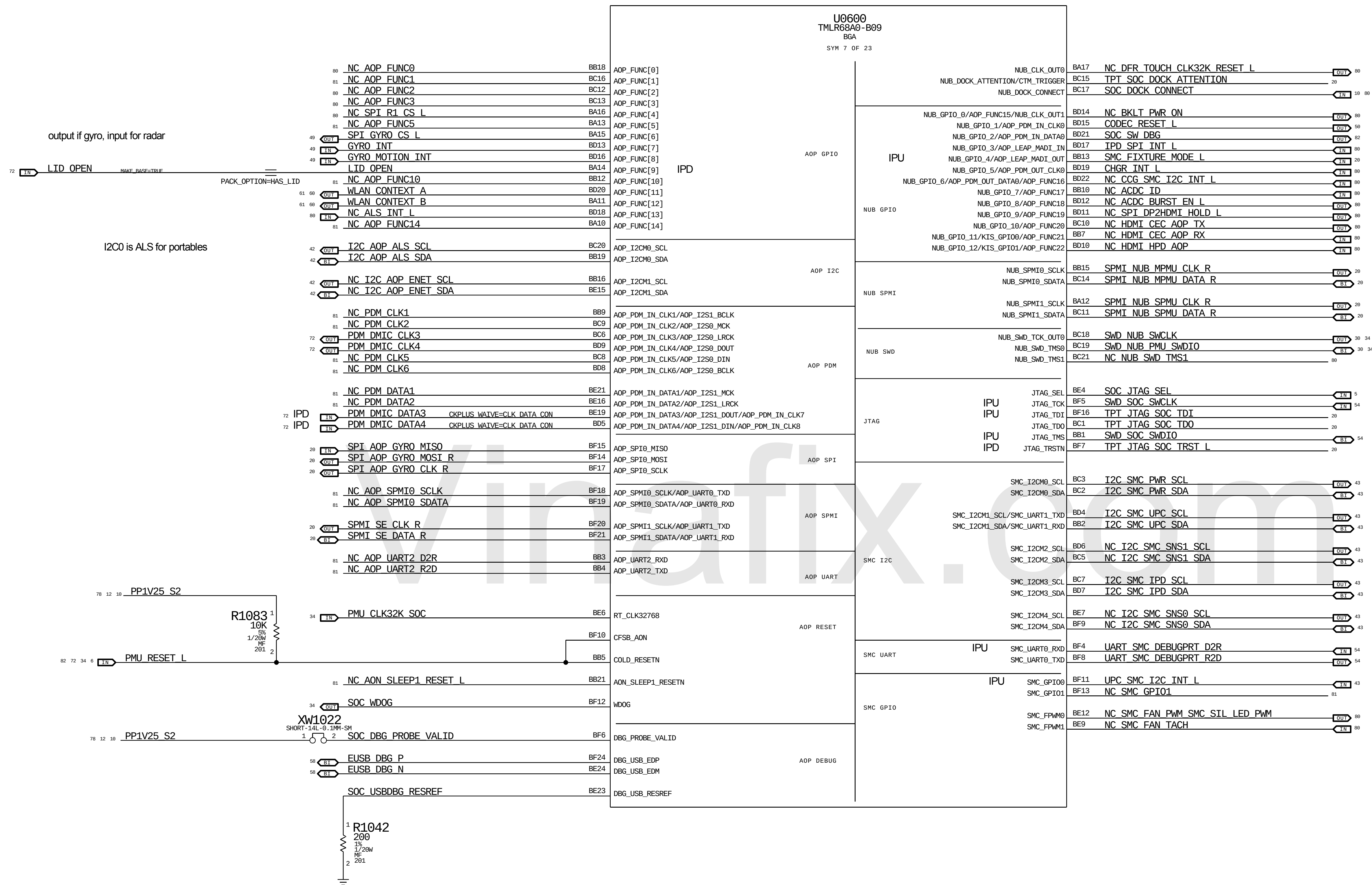
BOM_COST_GROUP=SOC

SOC: PCIE

OK2INTEGRATE

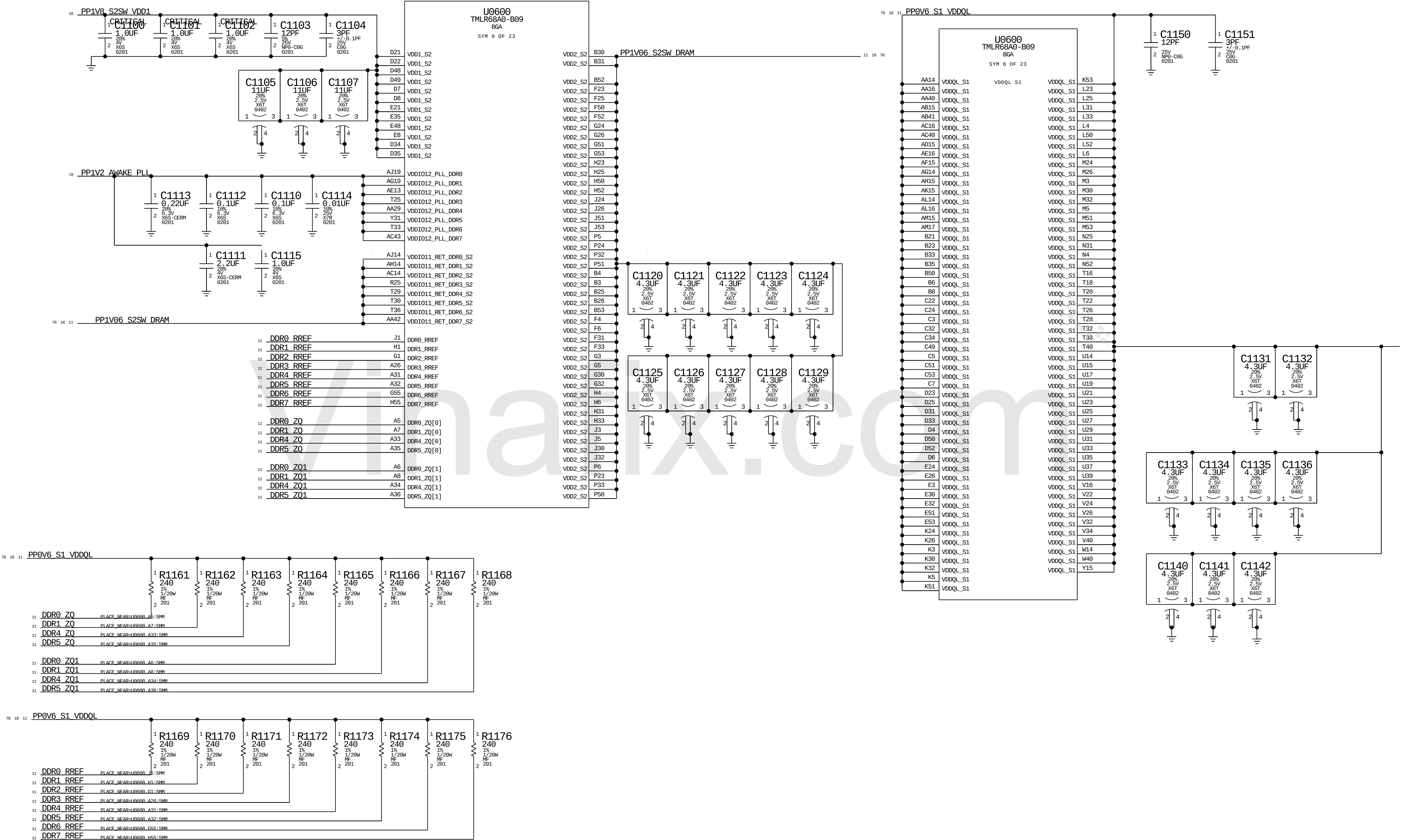
AOP, NUB, and SMC GPIO's are referenced to PP1V25_S2_AOP

SOC: AOP



SOC: POWER (DDR,SRAM)

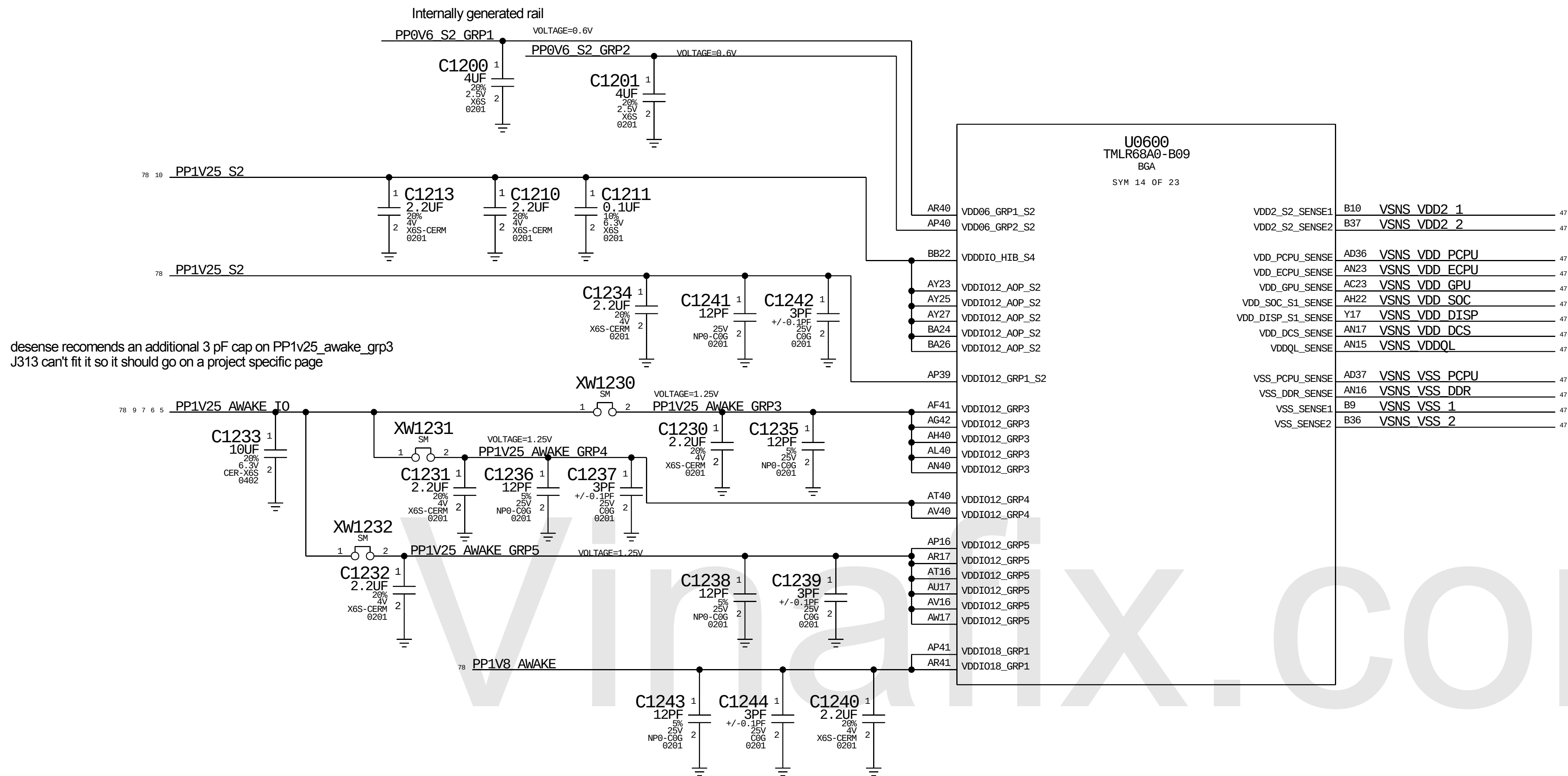
2		1		
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00139	138S00138		ALL	4.7UF 20% 4V 0201
138S00164	138S00138		ALL	4.7UF 20% 4V 0201



BOM_COST_GROUP=SOC

SOC: POWER (DDR,SRAM)

SOC: POWER (IO)



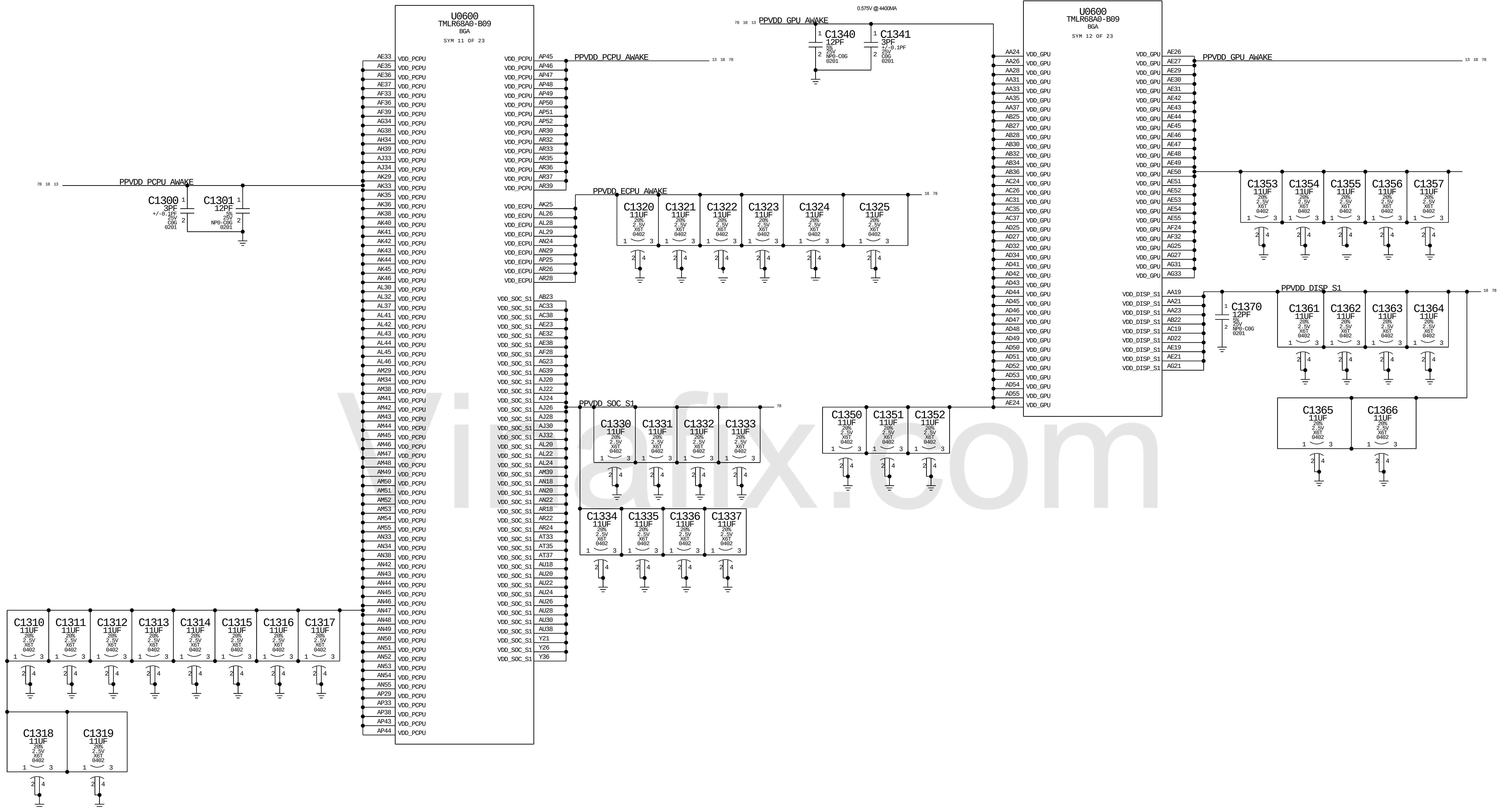
desense recommends an additional 3 pF cap on PP1v25_awake_grp3
J313 can't fit it so it should go on a project specific page

U0600
TMLR68A0-B09
BGA
SYM 14 OF 23

VDD2_S2_SENSE1	B10	VSNS_VDD2_1	47
VDD2_S2_SENSE2	B37	VSNS_VDD2_2	47
VDD_PCPU_SENSE	AD36	VSNS_VDD_PCPU	47
VDD_ECPU_SENSE	AN23	VSNS_VDD_ECPU	47
VDD_GPU_SENSE	AC23	VSNS_VDD_GPU	47
VDD_SOC_S1_SENSE	AH22	VSNS_VDD_SOC	47
VDD_DISP_S1_SENSE	Y17	VSNS_VDD_DISP	47
VDD_DCS_SENSE	AN17	VSNS_VDD_DCS	47
VDDQL_SENSE	AN15	VSNS_VDDQL	47
VSS_PCPU_SENSE	AD37	VSNS_VSS_PCPU	47
VSS_DDR_SENSE	AN16	VSNS_VSS_DDR	47
VSS_SENSE1	B9	VSNS_VSS_1	47
VSS_SENSE2	B36	VSNS_VSS_2	47

OK2INTEGRATE

SOC: POWER (CPU, GPU)

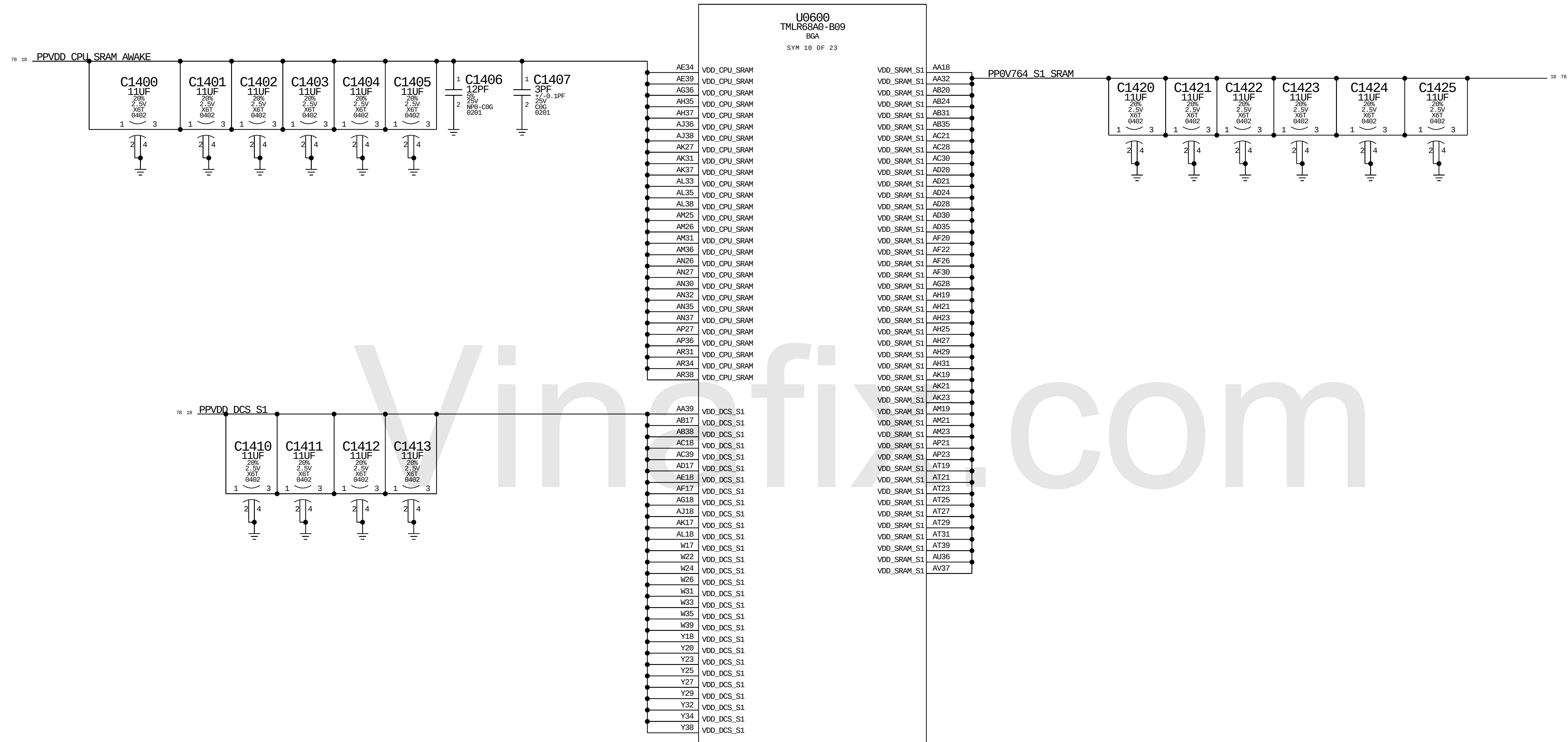


BOM_COST_GROUP=SOC

SOC: POWER (SOC, CPU, GPU)

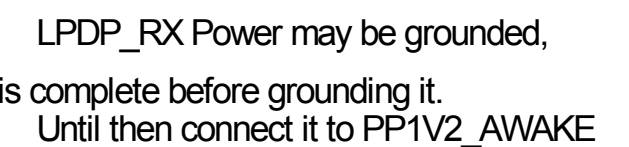
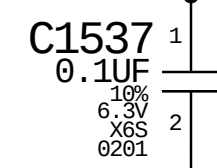
OK2INTEGRATE

SOC: POWER (SRAM, SOC)



SOC: POWER (SRAM)

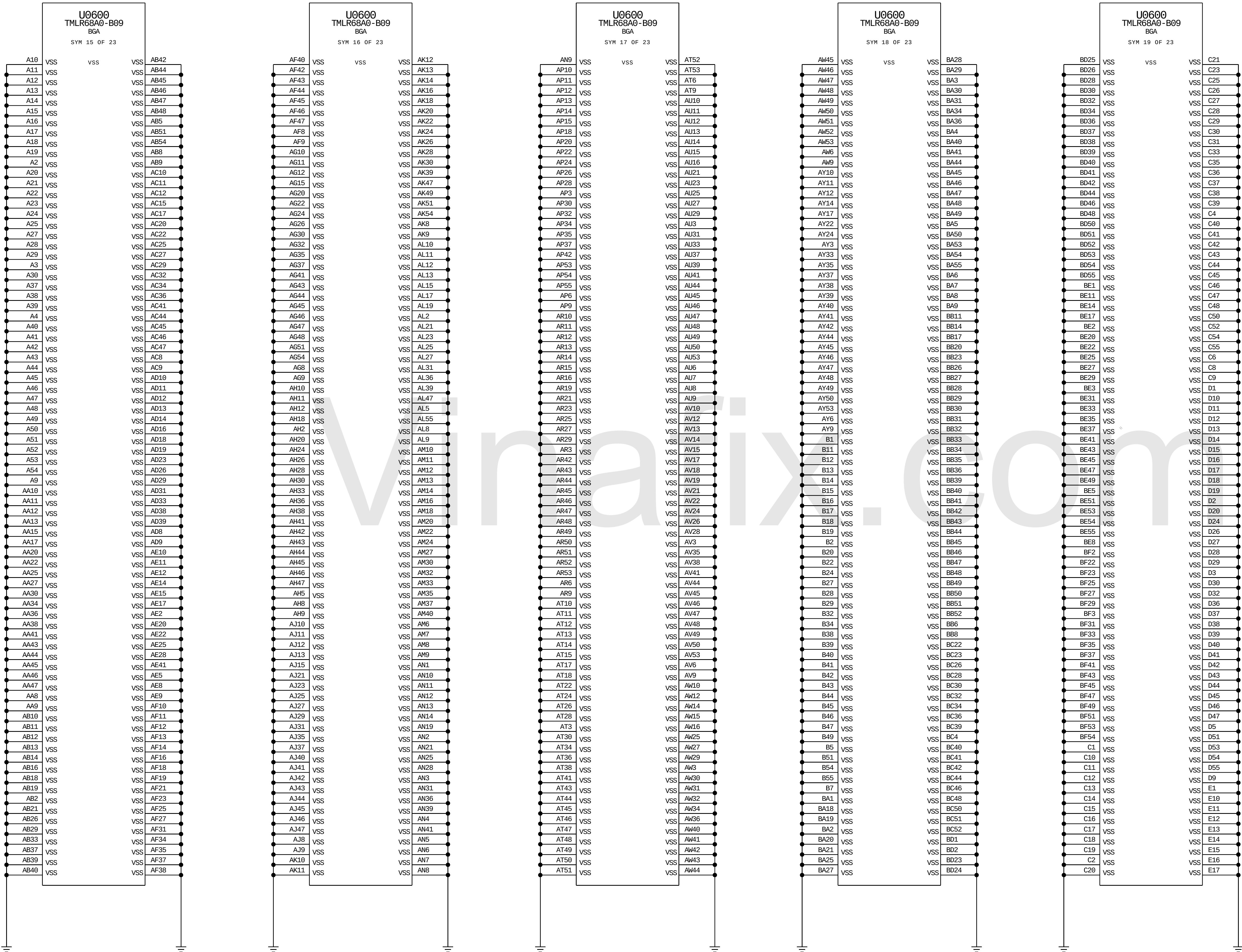
⁷⁸ PP0V805_S1_VDD_FIXED
LPDP_RX Power may be grounded,
Wait until Dev Bringup is complete before grounding it.
Until then connect it to PP1V2_AWAKE



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OK2INTEGRATE

SOC: GND (1)

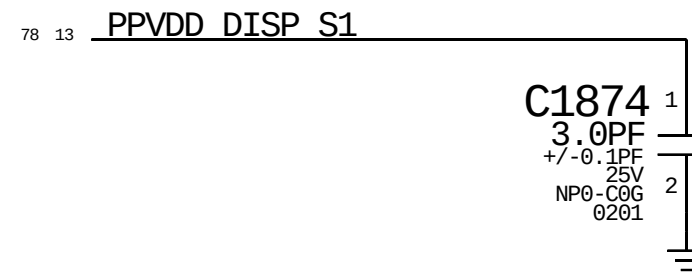
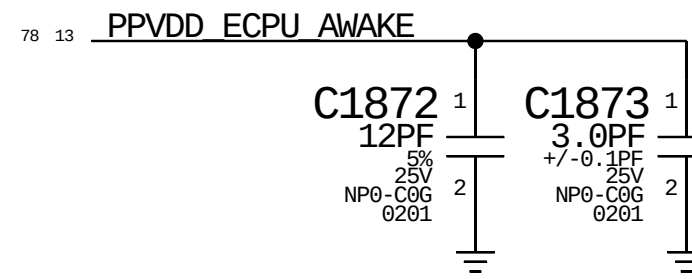
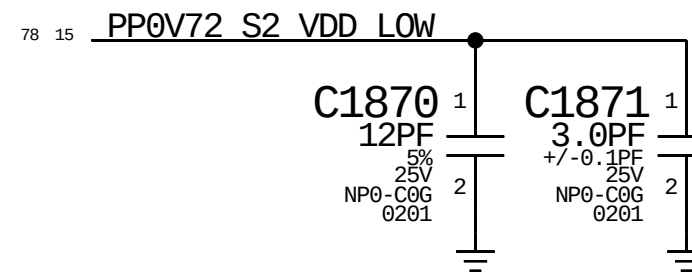
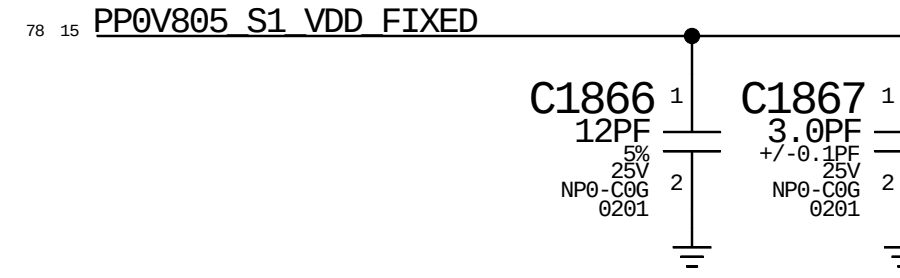
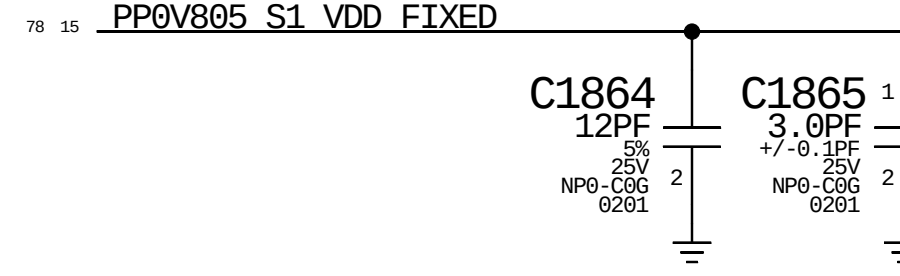
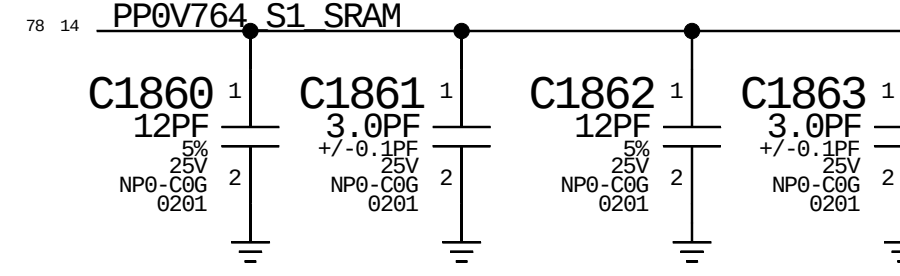
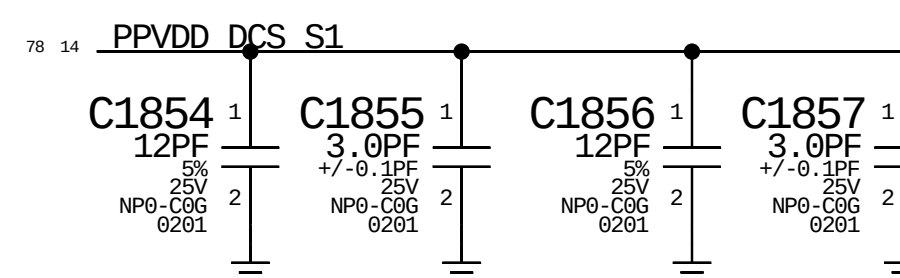
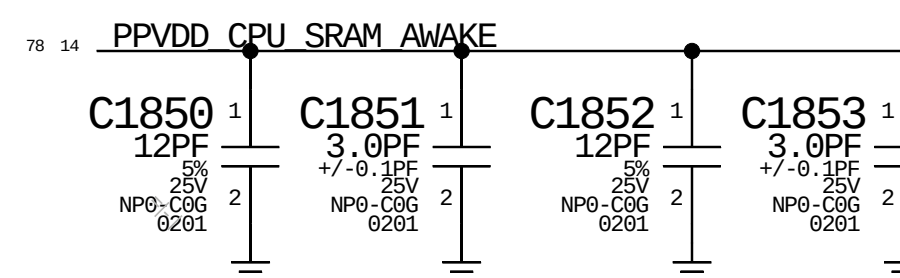
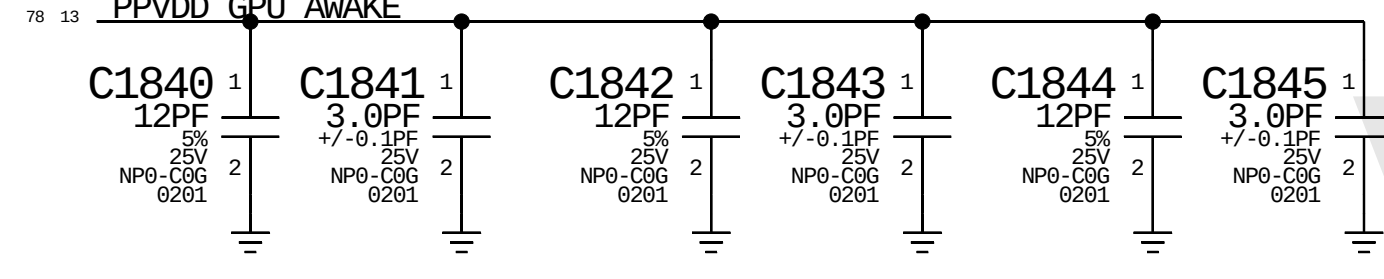
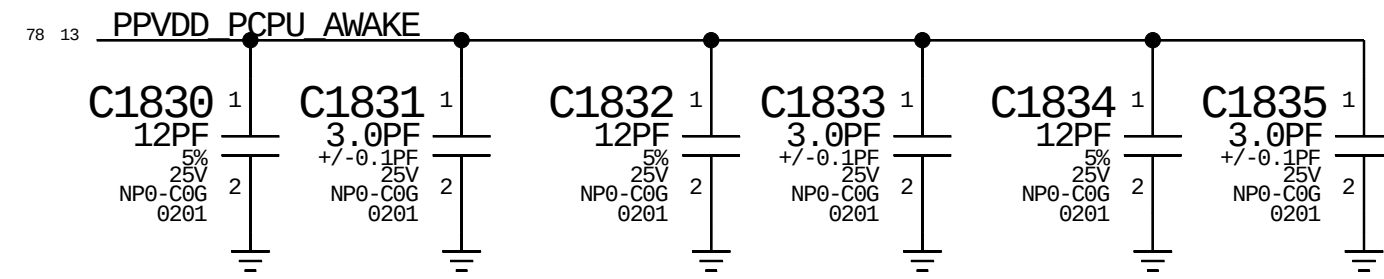
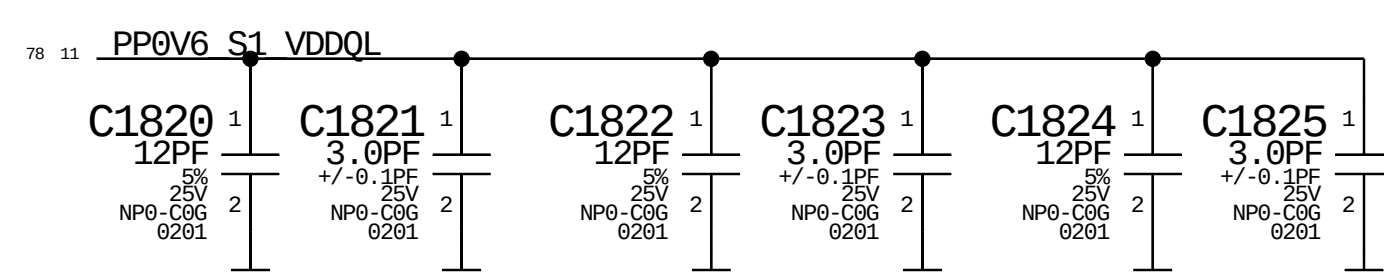
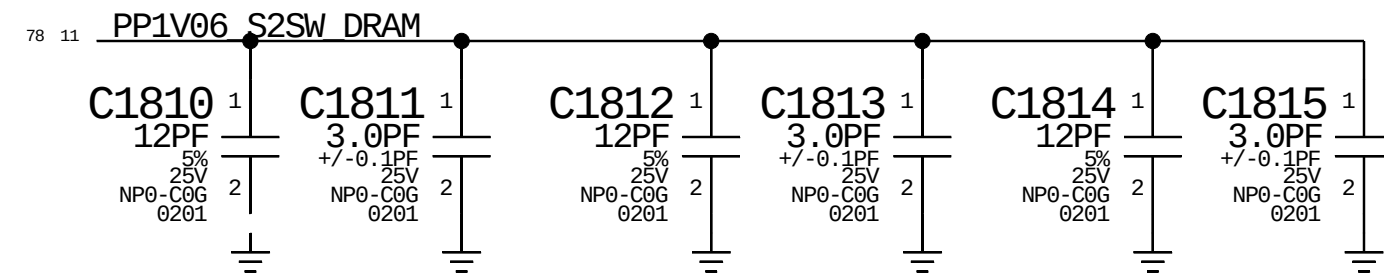
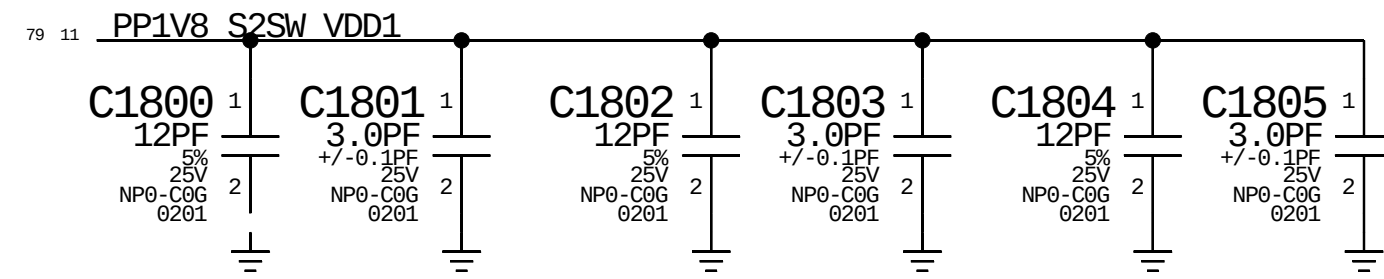


BOM_COST_GROUP=SOC

SOC: GND

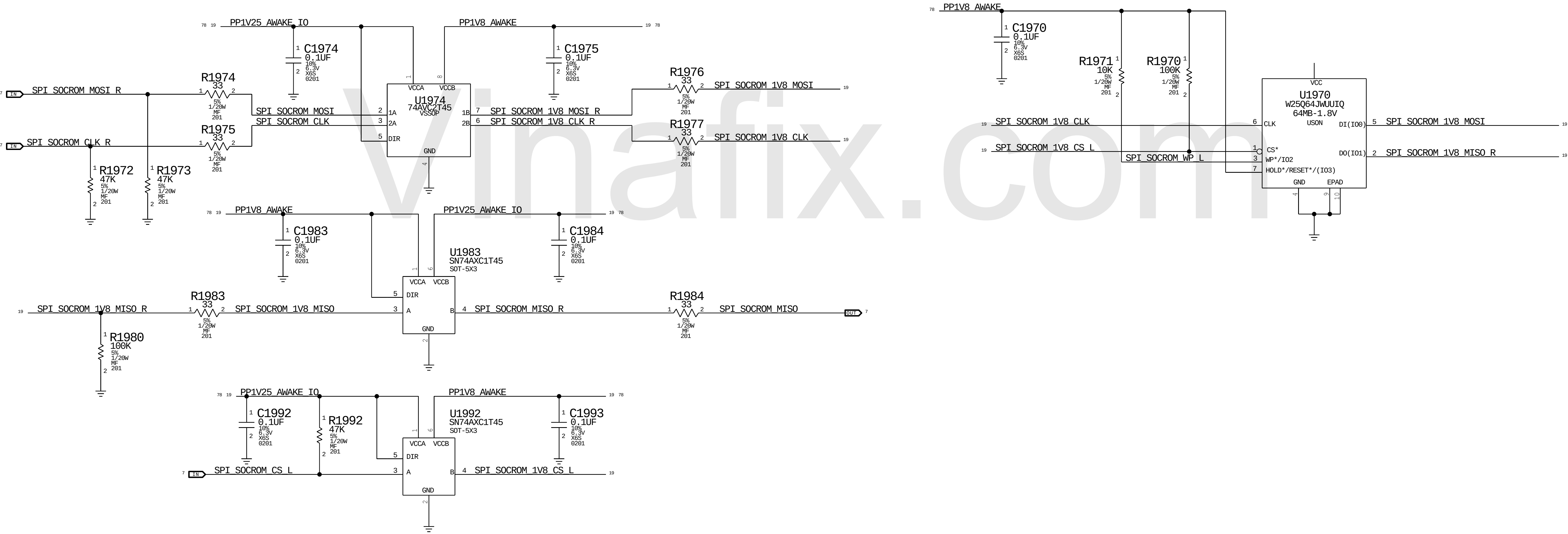
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	16	VSS	31	VSS	46	VSS
2	N21	17	R16	32	U3	47	Y13
3	VSS	18	VSS	33	U30	48	Y14
4	N22	19	VSS	34	VSS	49	VSS
5	VSS	20	R18	35	U32	50	Y16
6	N23	21	VSS	36	VSS	51	Y19
7	VSS	22	R19	37	U34	52	VSS
8	N24	23	VSS	38	VSS	53	Y22
9	VSS	24	R20	39	U36	54	VSS
10	N26	25	VSS	40	VSS	55	Y24
11	VSS	26	R21	41	U38	56	VSS
12	N27	27	VSS	42	VSS	57	Y28
13	VSS	28	R22	43	U4	58	VSS
14	N28	29	VSS	44	VSS	59	Y30
15	VSS	30	R23	45	U40	60	VSS
16	N29	31	VSS	46	VSS	61	Y35
17	VSS	32	R24	47	U41	62	VSS
18	N3	33	VSS	48	VSS	63	Y37
19	VSS	34	R26	49	U42	64	VSS
20	N30	35	VSS	50	VSS	65	Y39
21	VSS	36	R27	51	U43	66	VSS
22	N32	37	VSS	52	VSS	67	Y40
23	VSS	38	R3	53	U44	68	VSS
24	N33	39	VSS	54	VSS	69	Y41
25	VSS	40	R30	55	VSS		





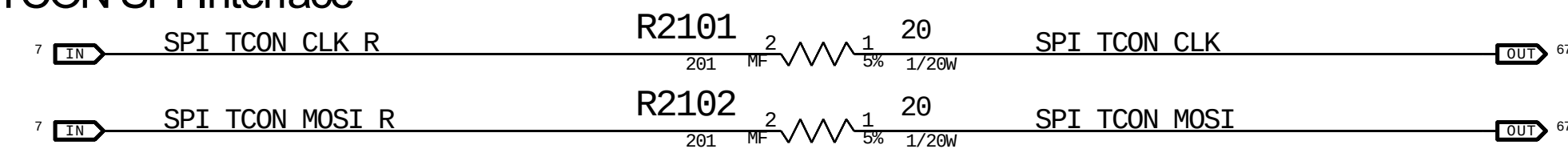
OK2INTEGRATE

SPI NOR (1.8V 64 M-BIT)

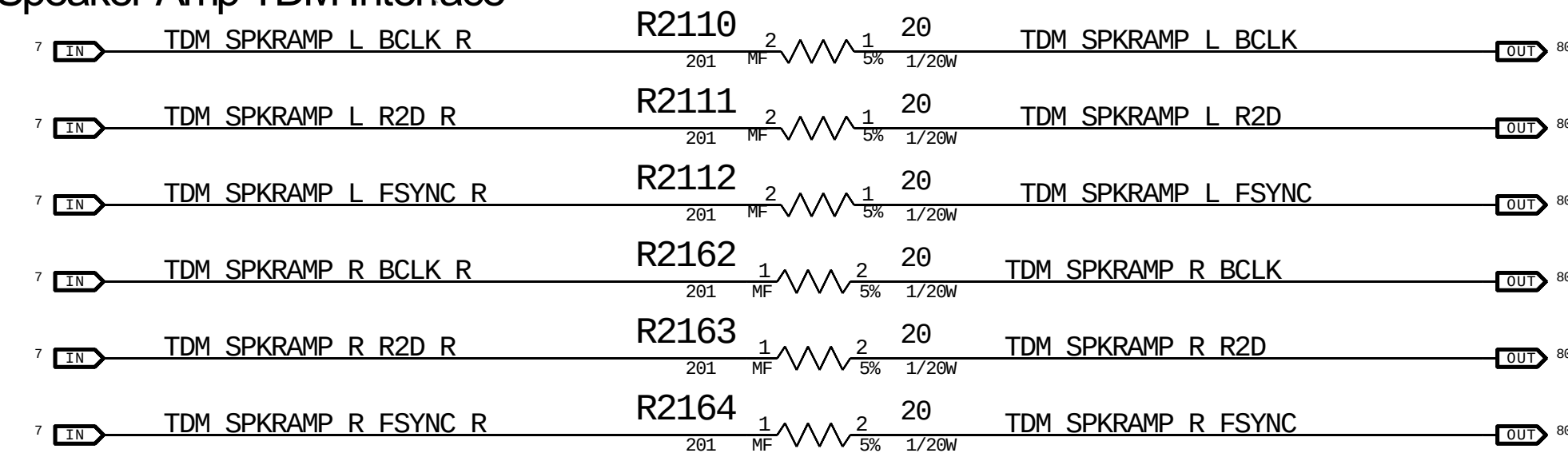


A Series Terminations

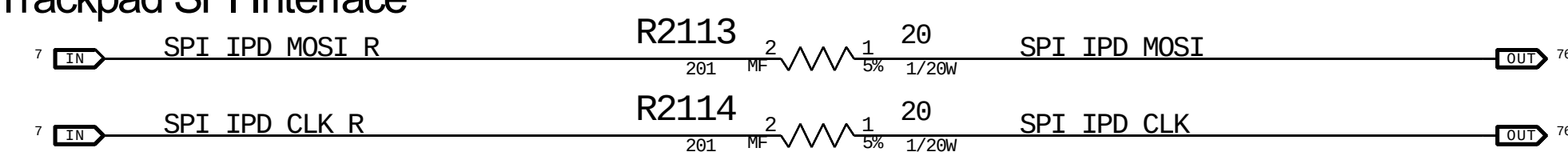
TCON SPI Interface



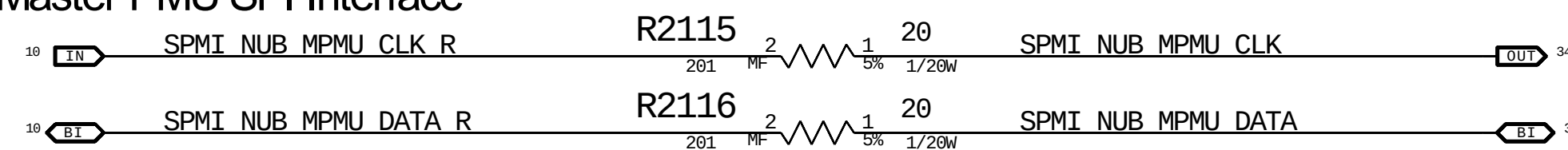
Speaker Amp TDM Interface



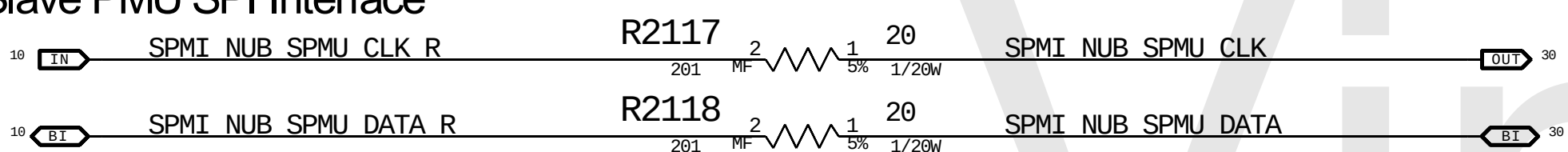
Trackpad SPI Interface



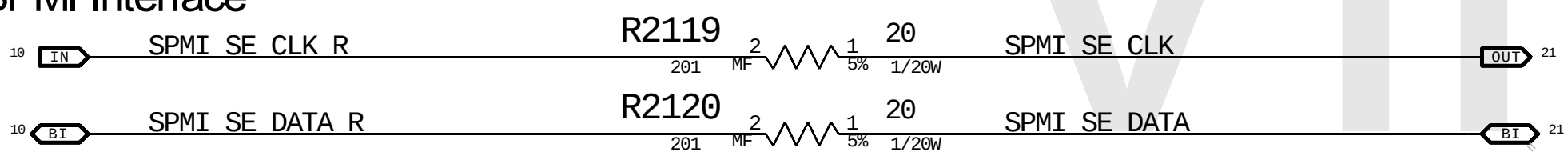
Master PMU SPI Interface



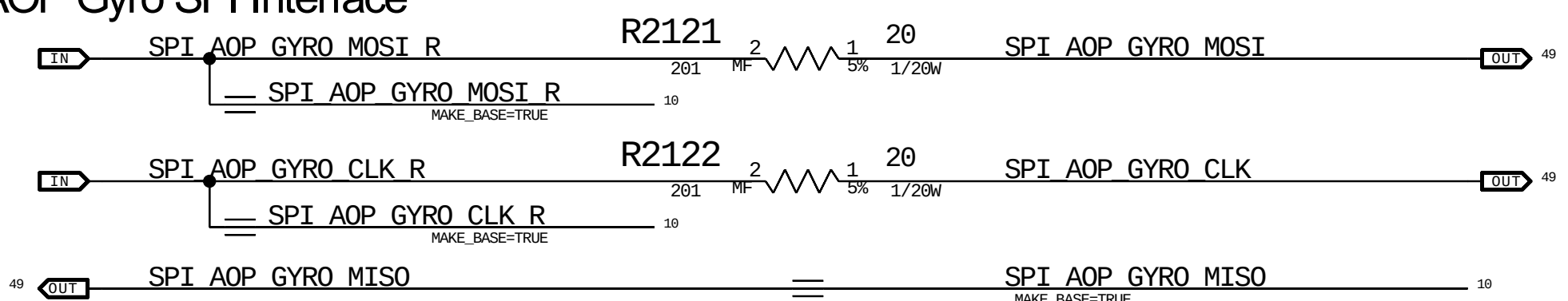
Slave PMU SPI Interface



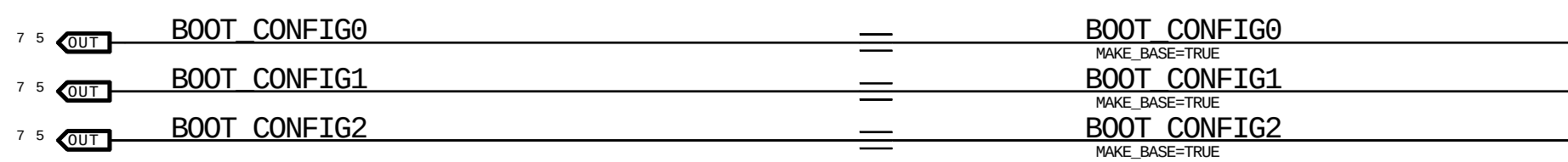
SPMI Interface



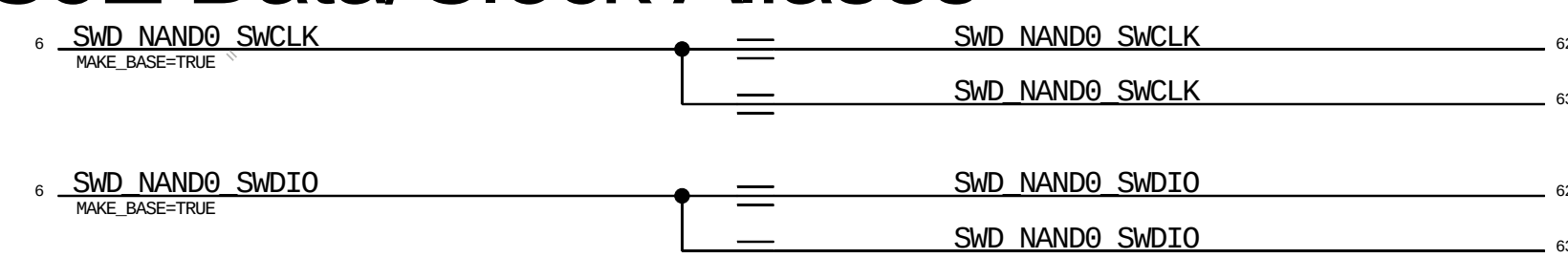
AOP Gyro SPI Interface



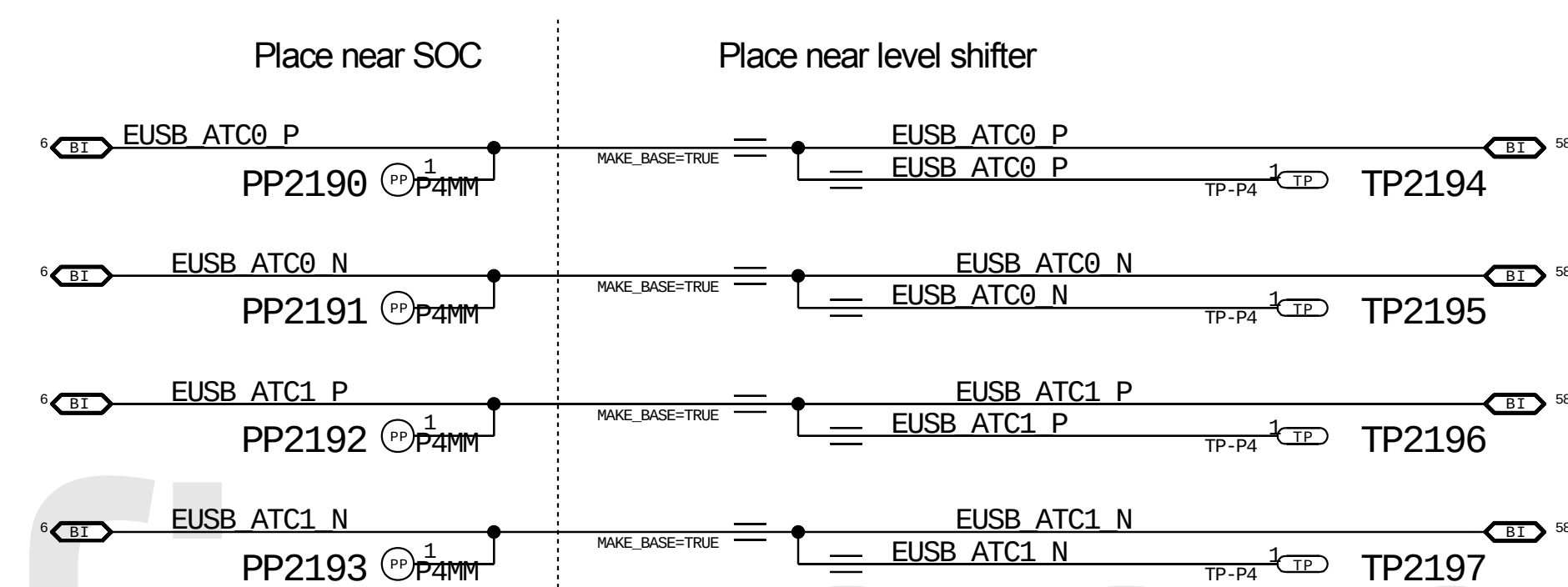
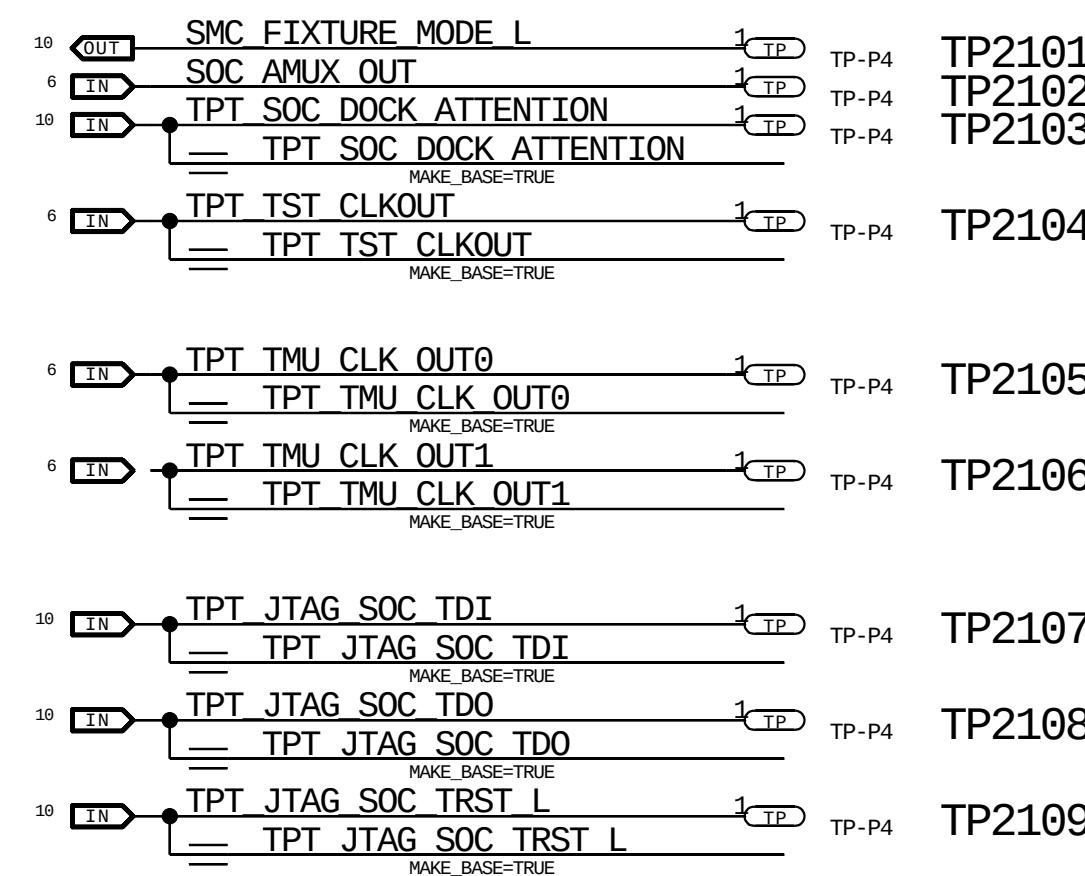
B BOOT Config Aliases



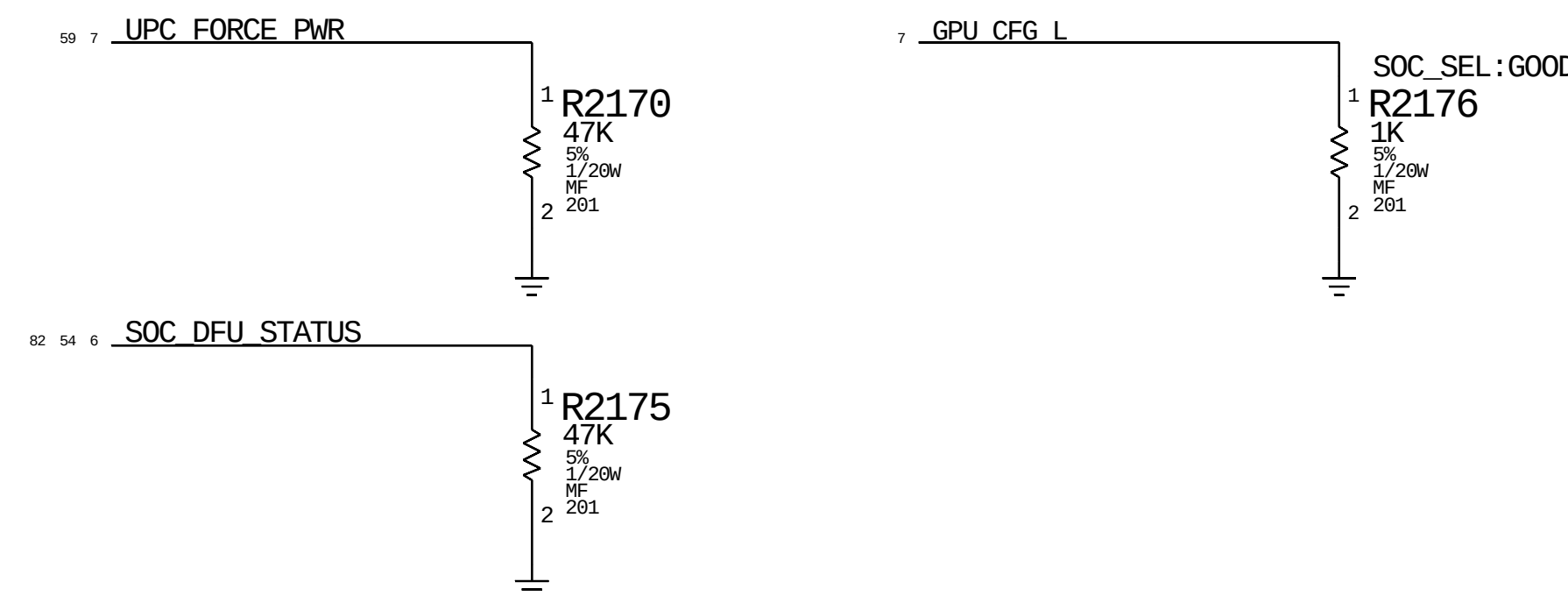
C SSD S5E Data/Clock Aliases



D Test Points



E Pull Down Resistors



- VBAT supply ramp time: 20ms

Ceres - Secure Element

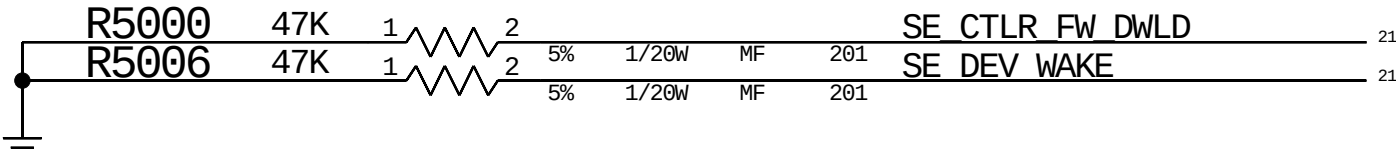
*** OK2INTEGRATE ***



Based on SPMI only use case

locMax: 100mA

As per NXP preliminary estimate, final pending



<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

Secure Element



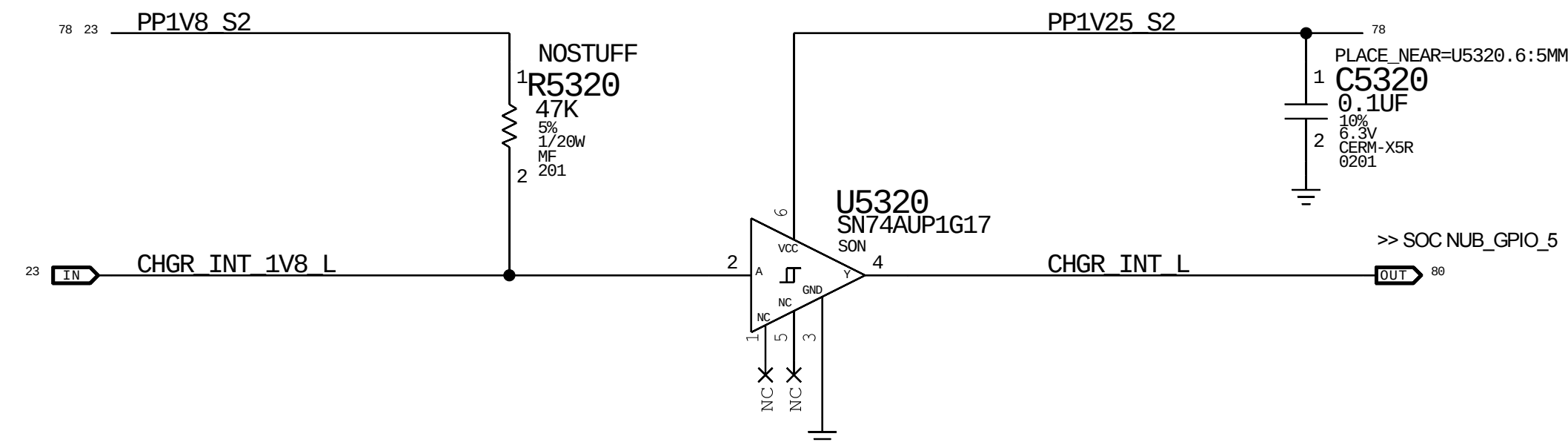
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.

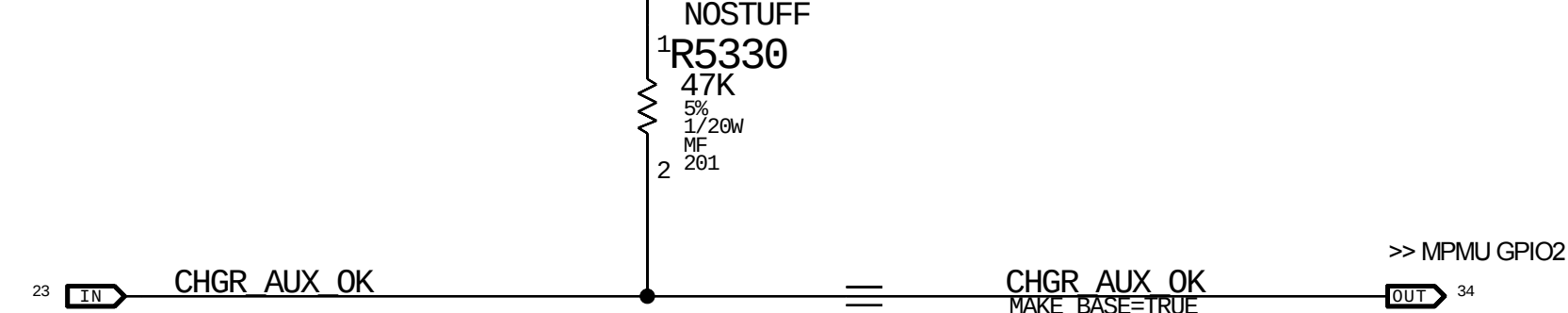


CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.

OK, to completely remove pull up, but consult PMU architecture and check OTP before that.

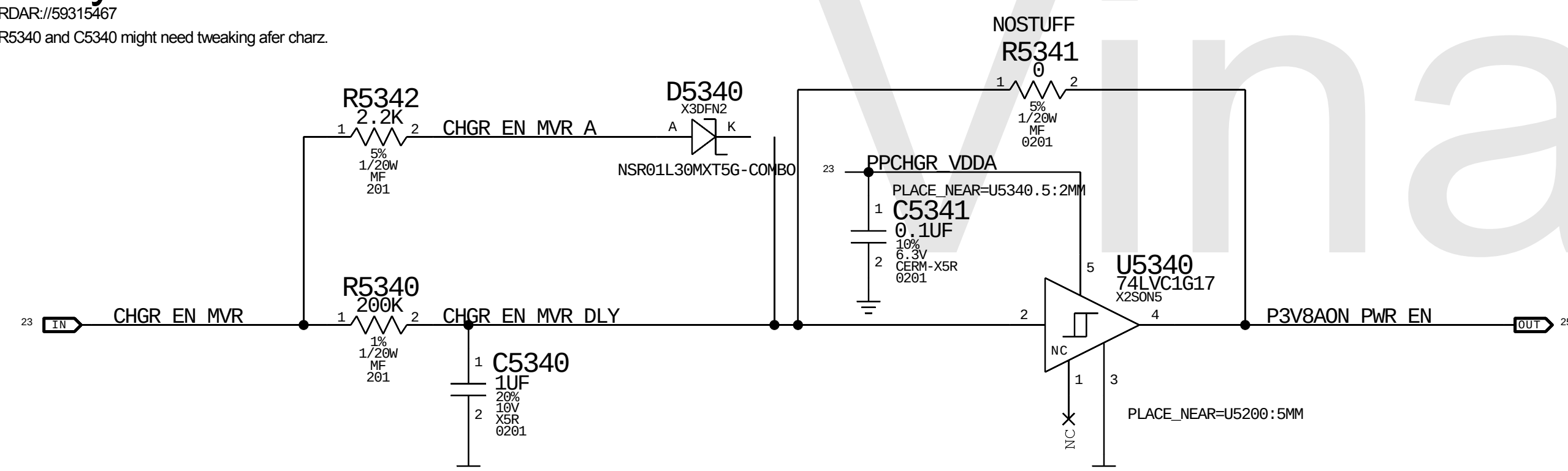
78 PP1V8 AON MPMU NOSTIFF



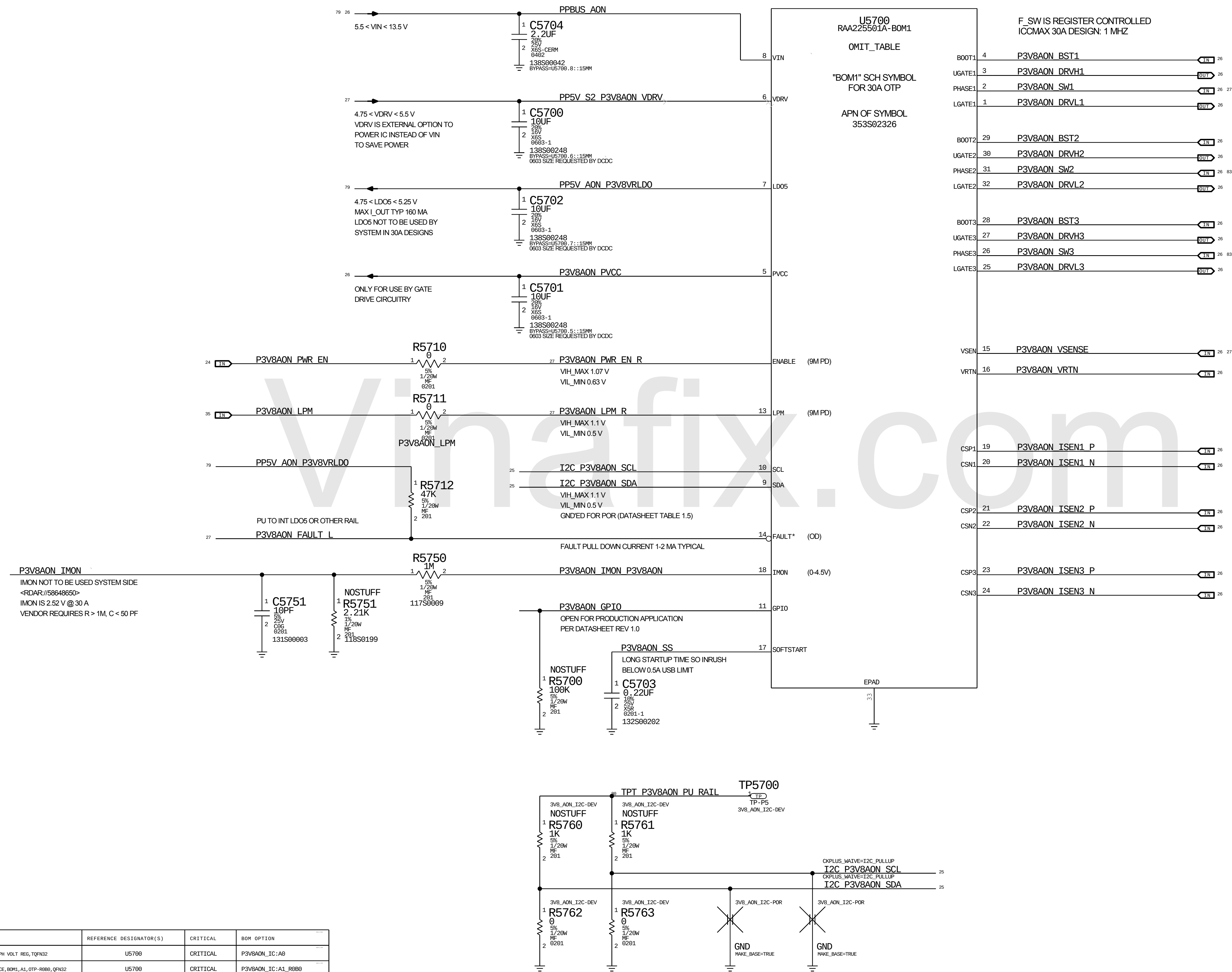
Delay for 3.8V VR Enable

RDAR://59315467

R5340 and C5340 might need tweaking after charz.



3V8 AON CONTROLLER



PAR#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S92326	1	IC, RAA225601, 3-PH VOLT REG, TQFN32	U5700	CRITICAL	P3V8A0N_IC:A0
353S92472	1	IC, RAA225601B, ICE, BOM1_A1, OTP-R800, QFN32	U5700	CRITICAL	P3V8A0N_IC:A1-R800

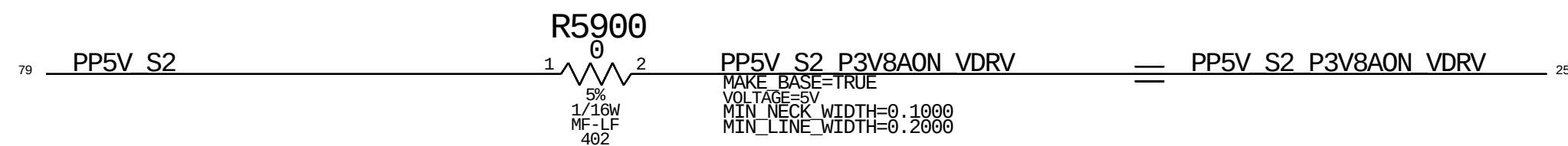
BOM_COST_GROUP=PLATFORM POWER

POWER: 3V8 A0N (1/2)

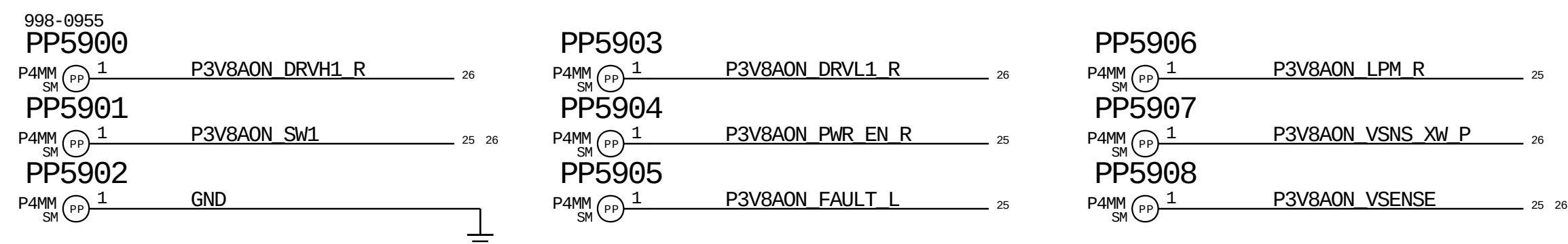


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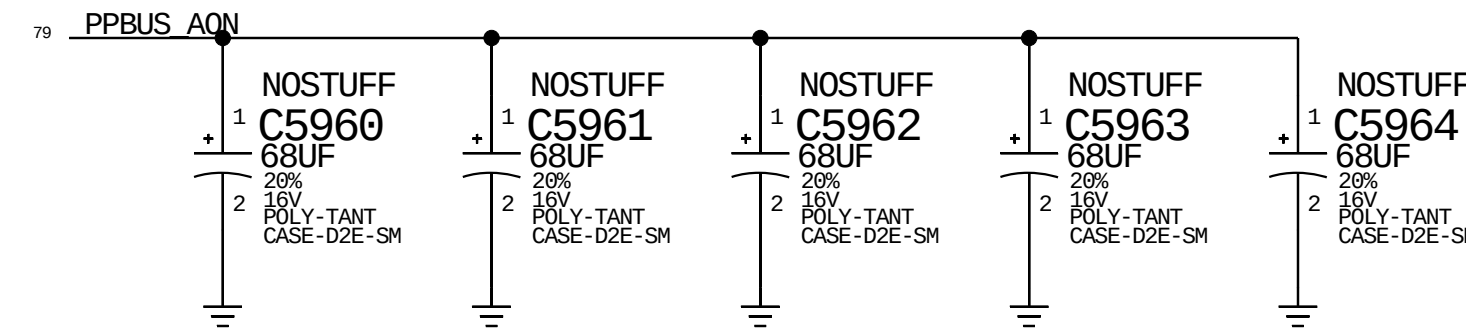
A PP5V_S2 to PP3V8_AON VDRV Connection



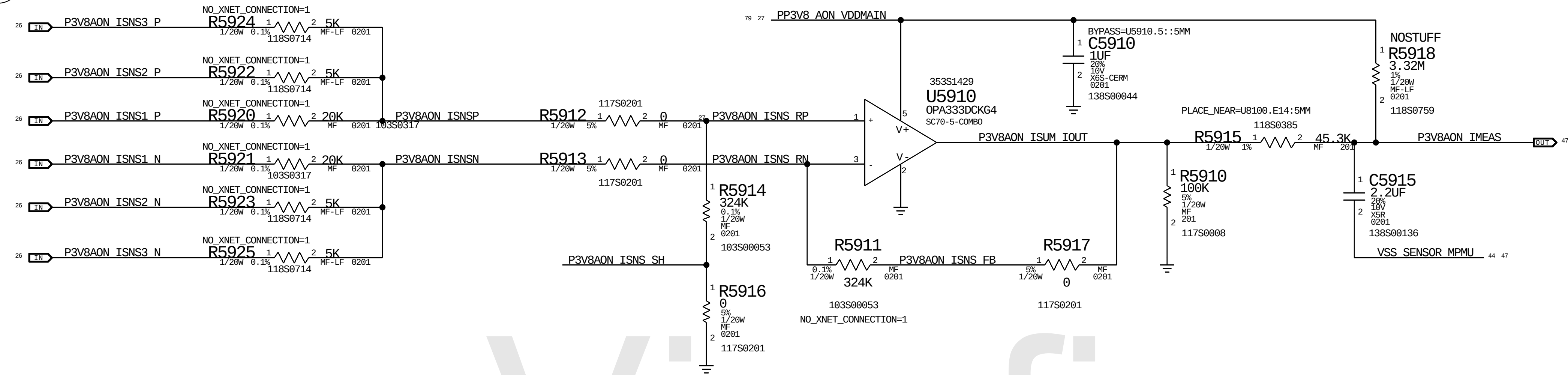
B PP3V8_AON Probe Points



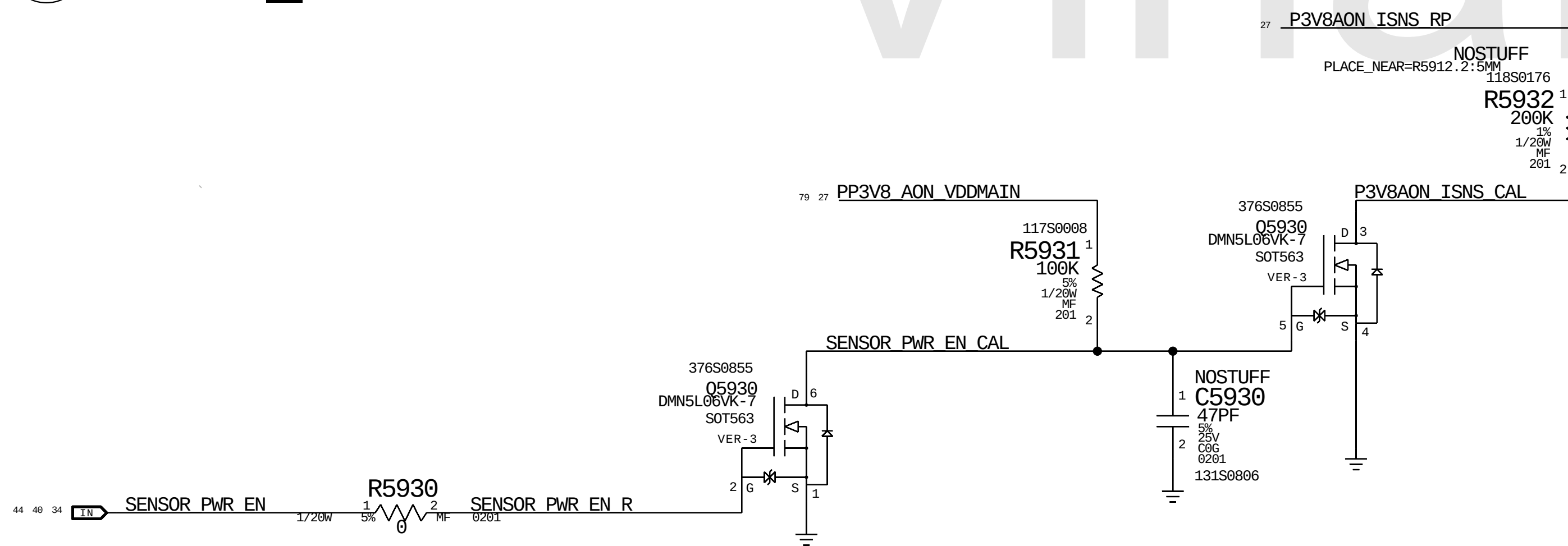
C PPBUS_AON Bulk Capacitance



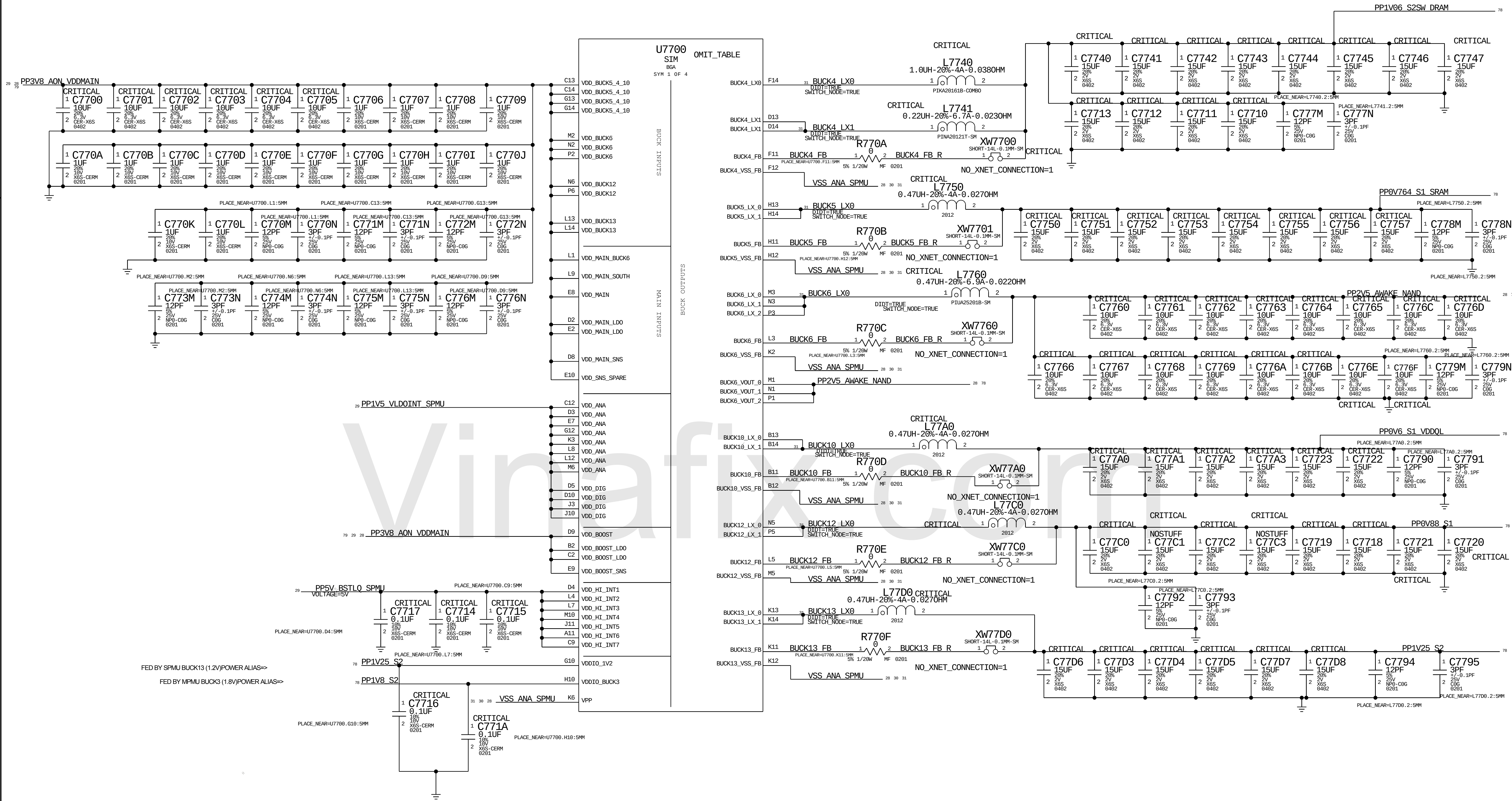
D PP3V8_AON Current Sense



E PP3V8_AON Current Sense Cal Control Circuit



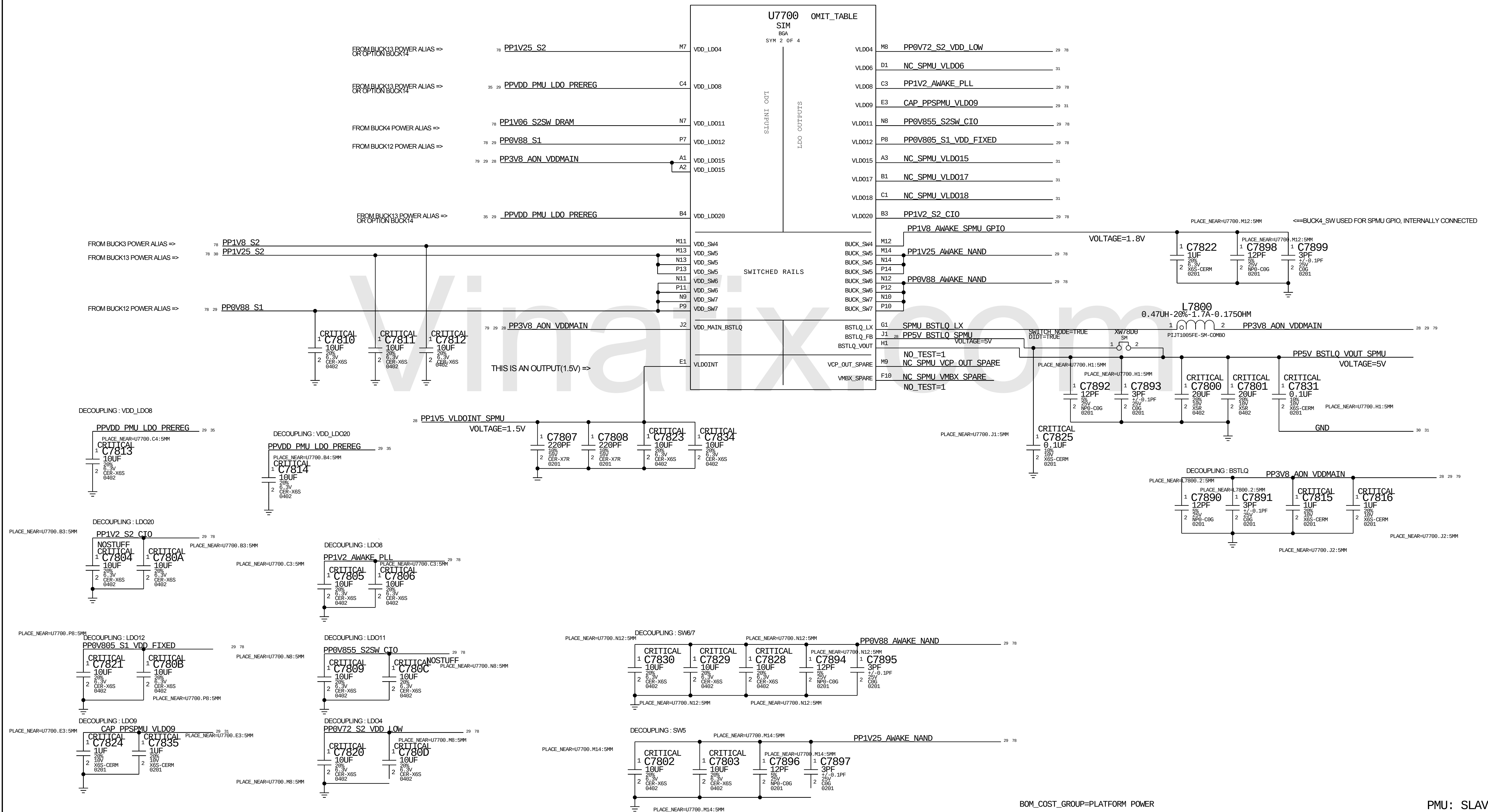
SLAVE PMU BUCKS



SLAVE PMU LDO

LDO INPUTS

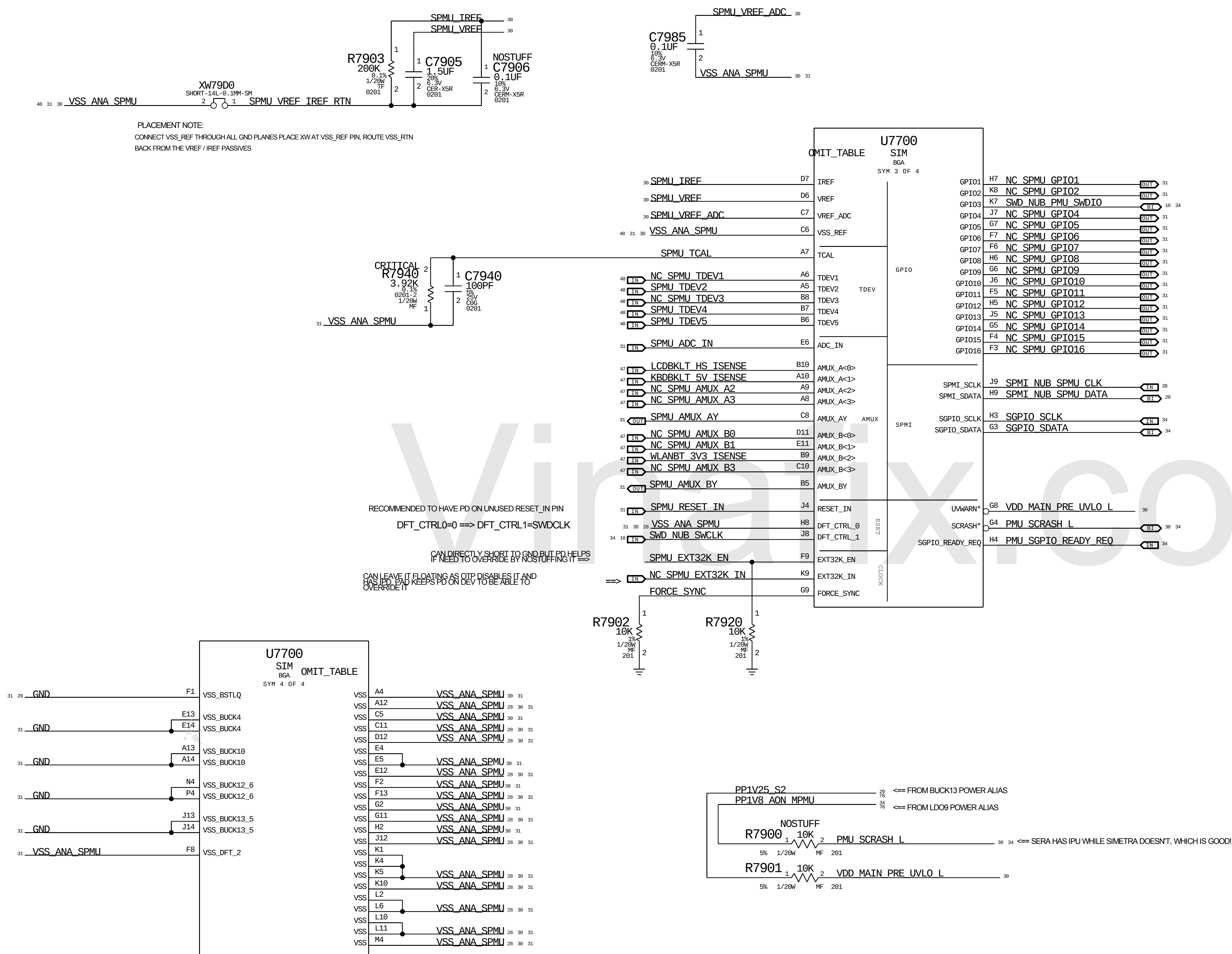
LDO OUTPUTS



BOM_COST_GROUP=PLATFORM POWER

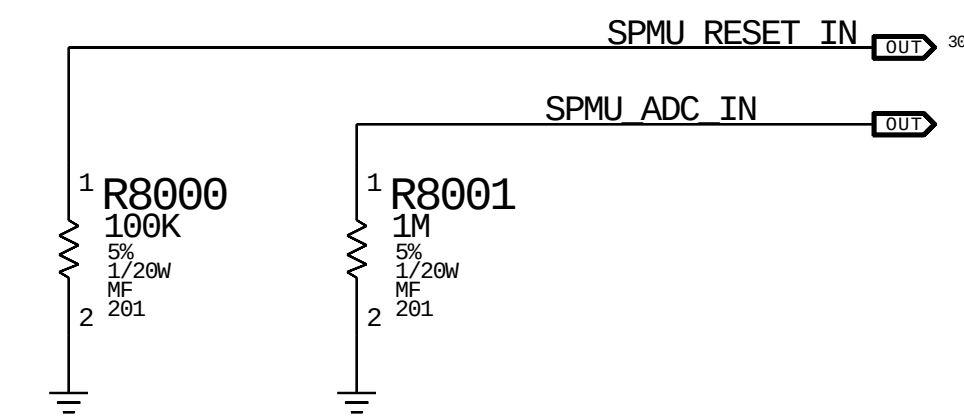
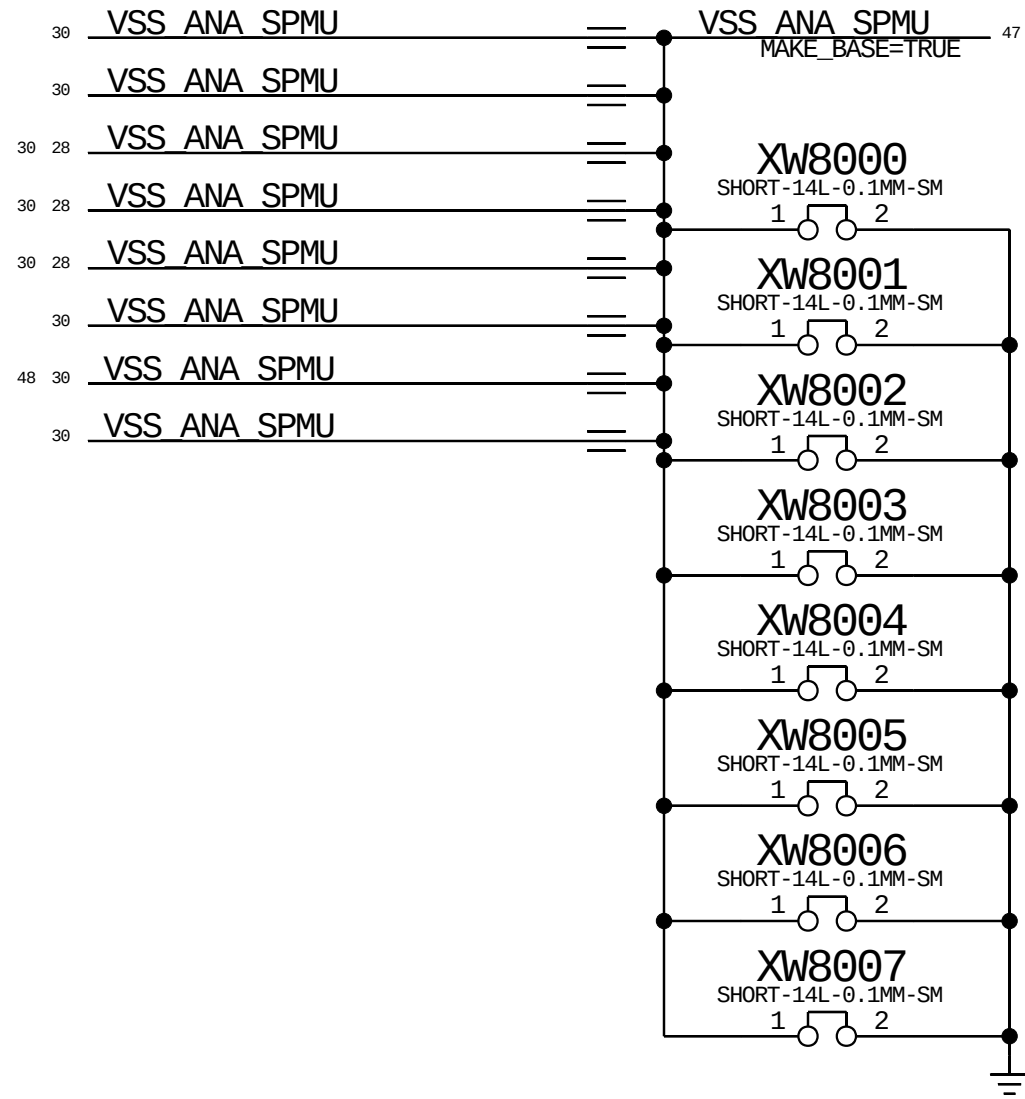
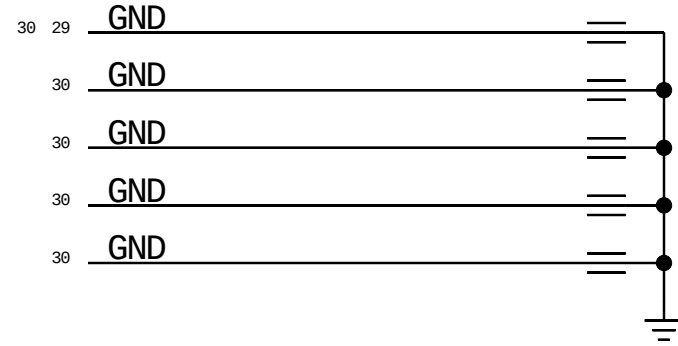
PMU: SLAVE LDO

SLAVE PMU GND,ADC,& GPIO

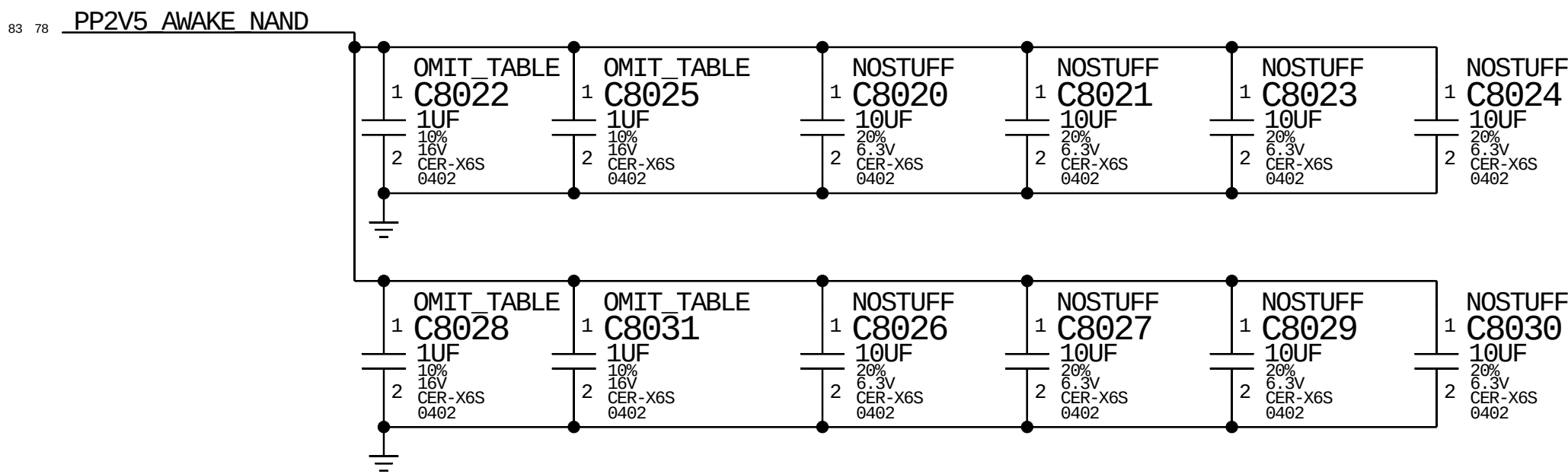
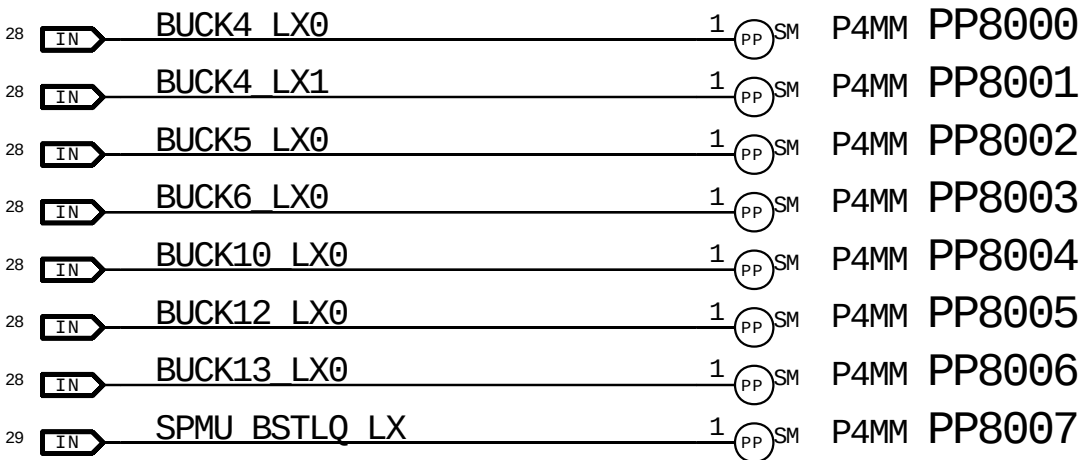
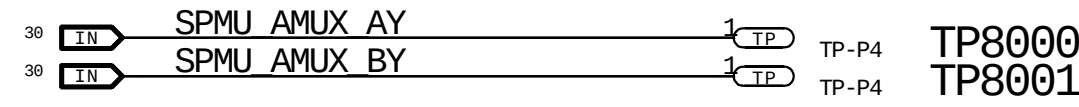


BOM_COST_GROUP=PLATFORM POWER

PMU: SLAVE GPIO & GND



NC SPMU VLD06	==	NC SPMU VLD06	==	MAKE_BASE=TRUE	NO_TEST=1
CAP_PPSPMU VLD09	==	CAP_PPSPMU VLD09	==	MAKE_BASE=TRUE	
NC SPMU VLD015	==	NC SPMU VLD015	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU VLD017	==	NC SPMU VLD017	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU VLD018	==	NC SPMU VLD018	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU EXT32K IN	==	NC SPMU EXT32K IN	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO1	==	NC SPMU GPIO1	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO2	==	NC SPMU GPIO2	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO4	==	NC SPMU GPIO4	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO5	==	NC SPMU GPIO5	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO6	==	NC SPMU GPIO6	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO7	==	NC SPMU GPIO7	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO8	==	NC SPMU GPIO8	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO9	==	NC SPMU GPIO9	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO10	==	NC SPMU GPIO10	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO11	==	NC SPMU GPIO11	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO12	==	NC SPMU GPIO12	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO13	==	NC SPMU GPIO13	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO14	==	NC SPMU GPIO14	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO15	==	NC SPMU GPIO15	==	MAKE_BASE=TRUE	NO_TEST=1
NC SPMU GPIO16	==	NC SPMU GPIO16	==	MAKE_BASE=TRUE	NO_TEST=1

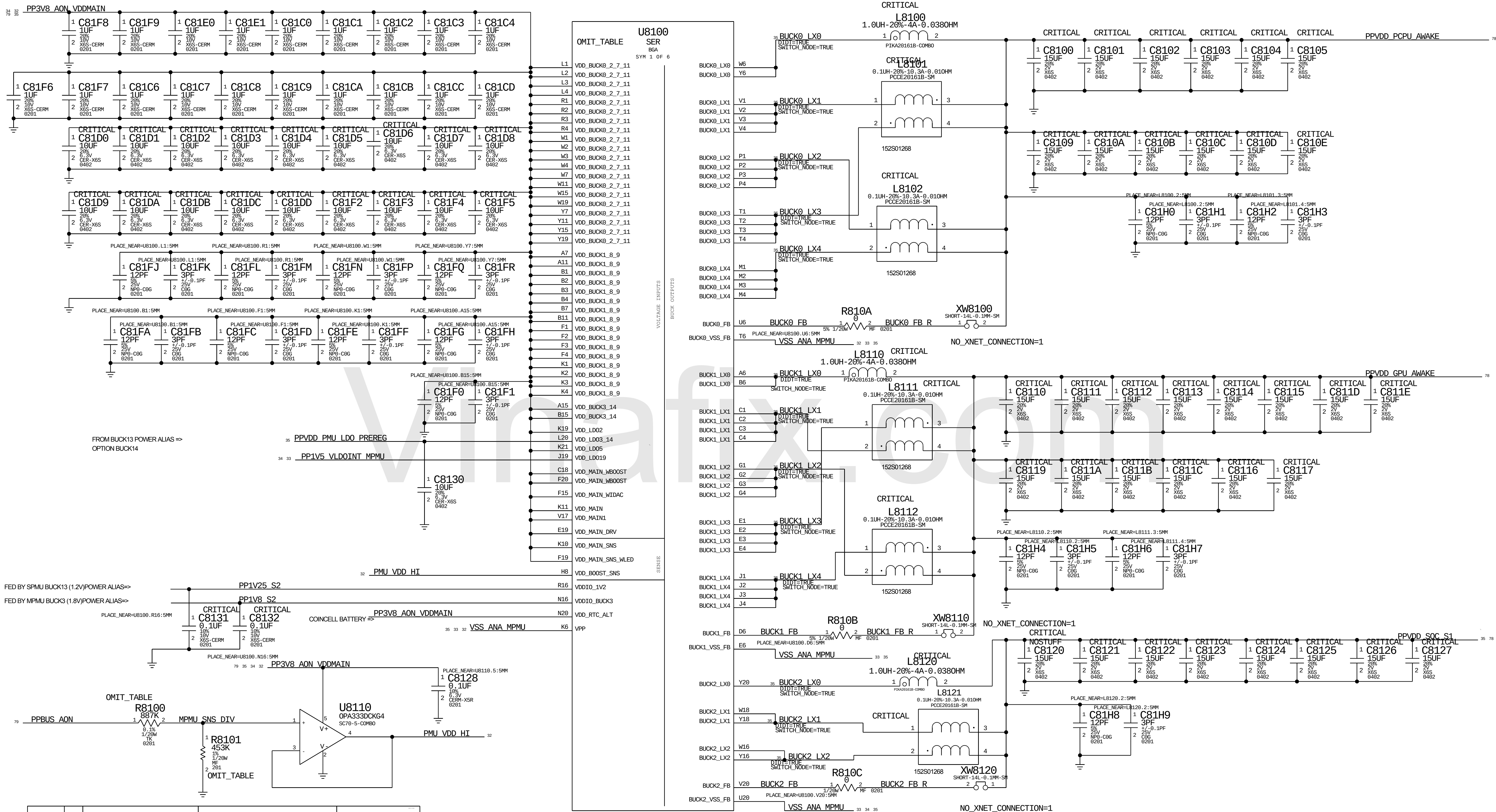


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138s00336	5	CAP, CER, 10F, 10%, 16V, X6S, MUR, 0402	C5151, C8022, C8025, C8026, C8031		

BOM_COST_GROUP=PLATFORM POWER

PMU: Slave extra

MASTER PMU BUCKS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
183S00385	1	RES, TK, 887KOHM, 0.1%, 1/20W, 0201	R8100	CRITICAL	PBUS_3S
183S00480	1	RES, MF, 453KOHM, 0.1%, 1/20W, 0201	R8101	CRITICAL	PBUS_3S
183S00481	1	RES, MF, 910KOHM, 0.1%, 1/20W, 0201	R8100	CRITICAL	PBUS_12VDCIN
183S00643	1	RES, MF, 280KOHM, 0.1%, 1/20W, 0201	R8101	CRITICAL	PBUS_12VDCIN
183S00385	1	RES, TK, 887KOHM, 0.1%, 1/20W, 0201	R8100	CRITICAL	PBUS_15P8VDCIN
183S00606	1	RES, MF, 205KOHM, 0.1%, 1/20W, 0201	R8101	CRITICAL	PBUS_15P8VDCIN

<== FOR 3S BATTERY

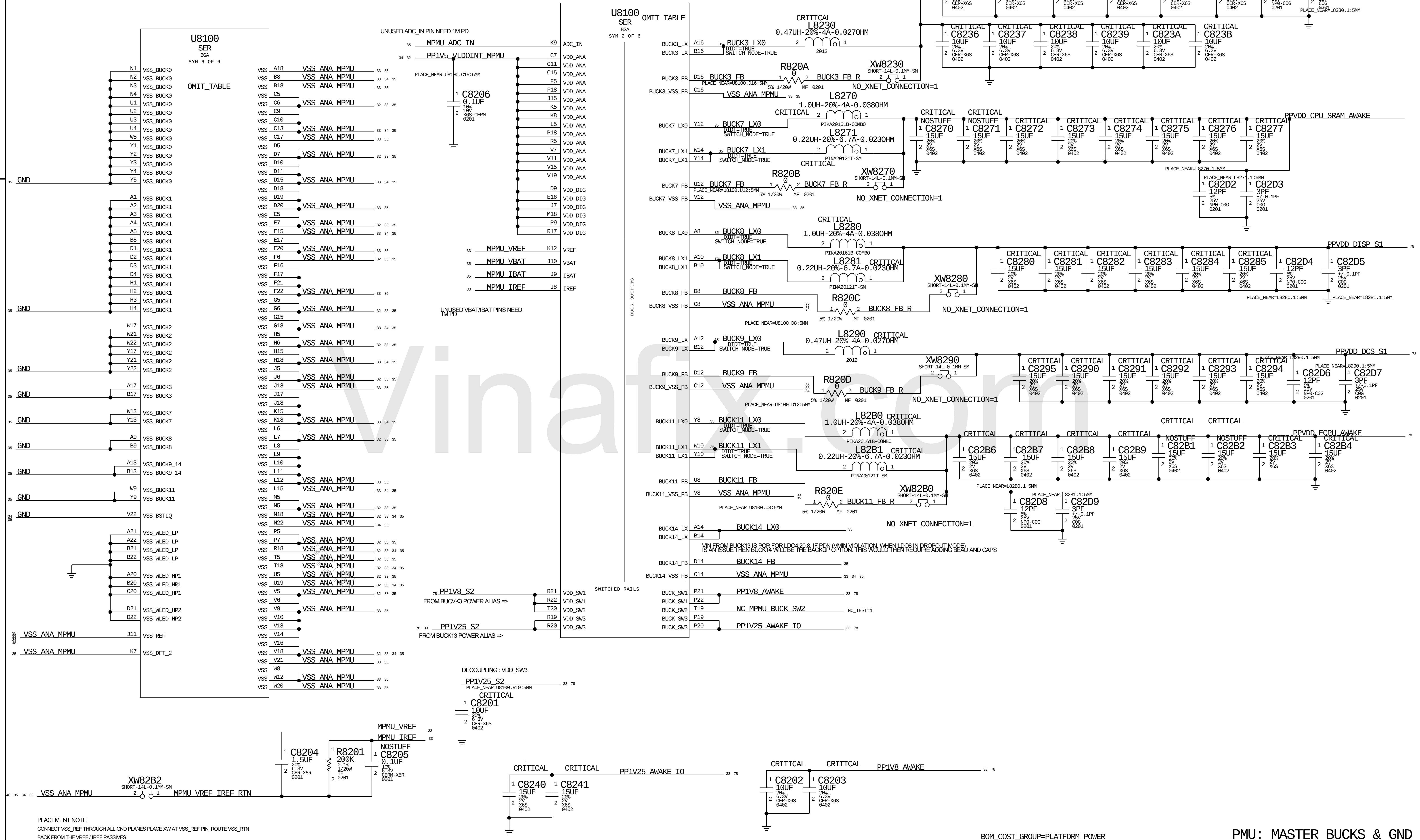
<== FOR 12V DCIN

<== FOR 15.8V DCIN

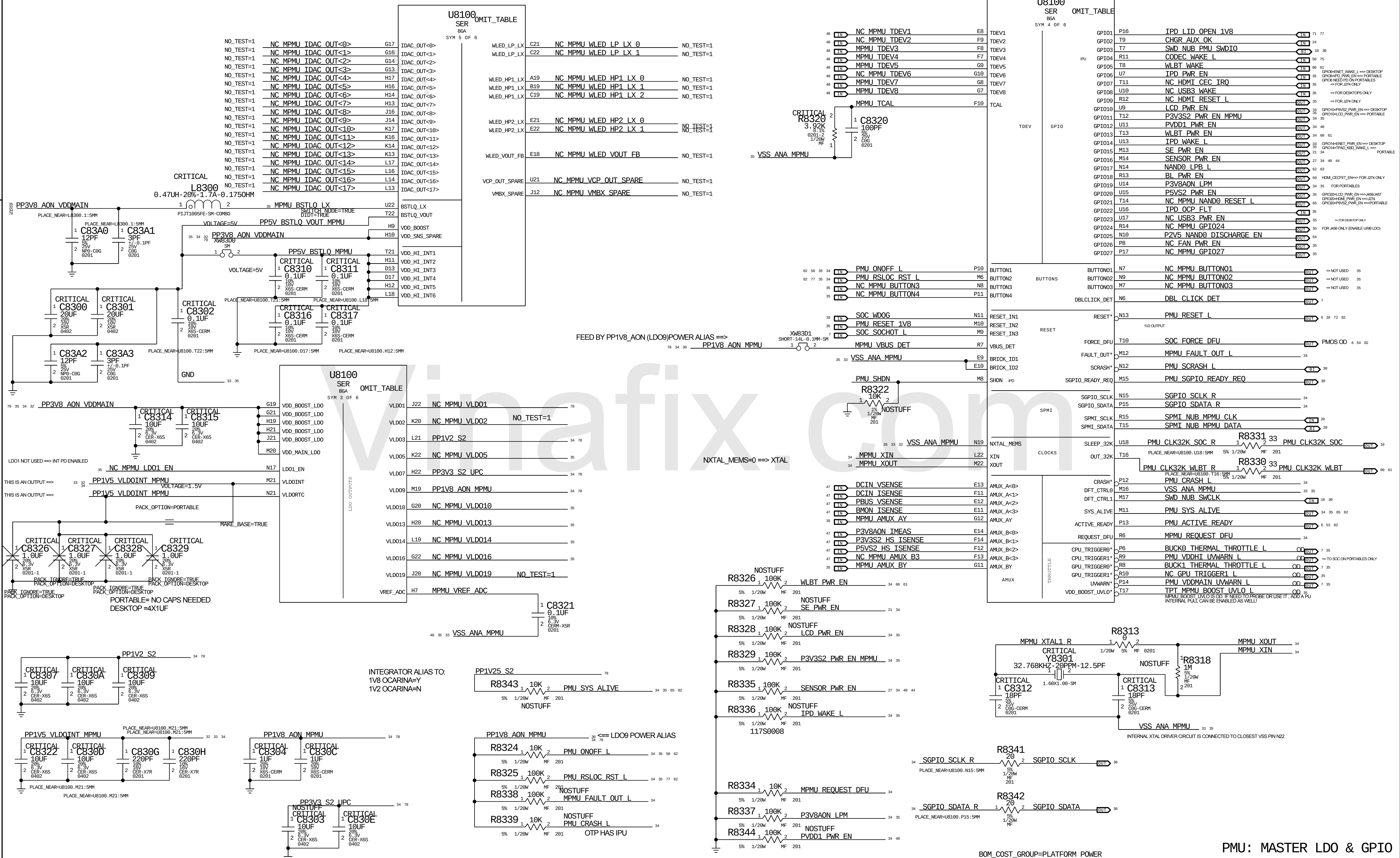
BOM_COST_GROUP=PLATFORM POWER

PMU: MASTER INPUT PWR & BUCKS

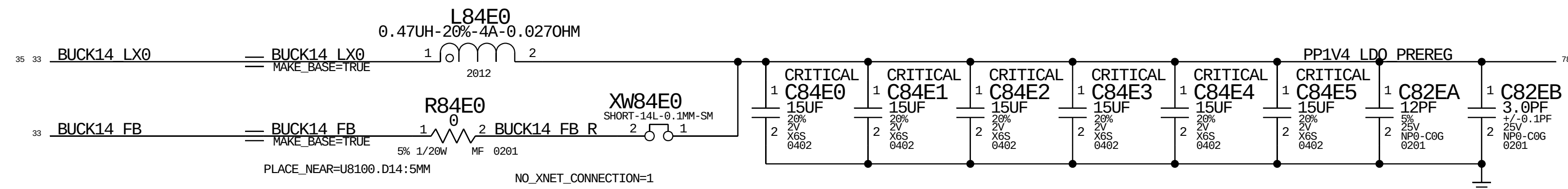
MASTER PMU BUCKS & GND



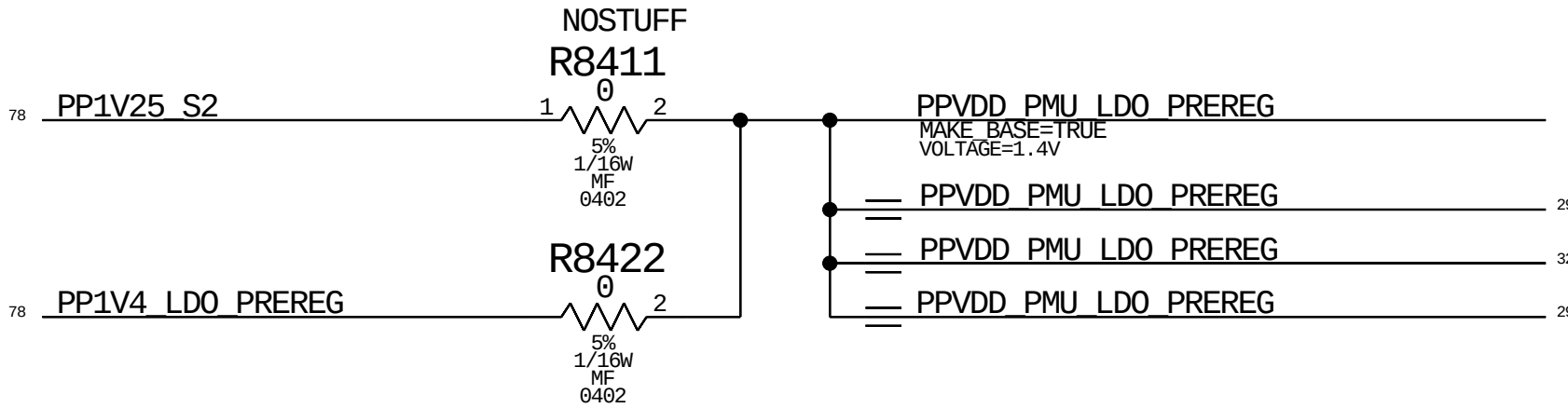
MASTER PMU LDO, ADC, & GPIO



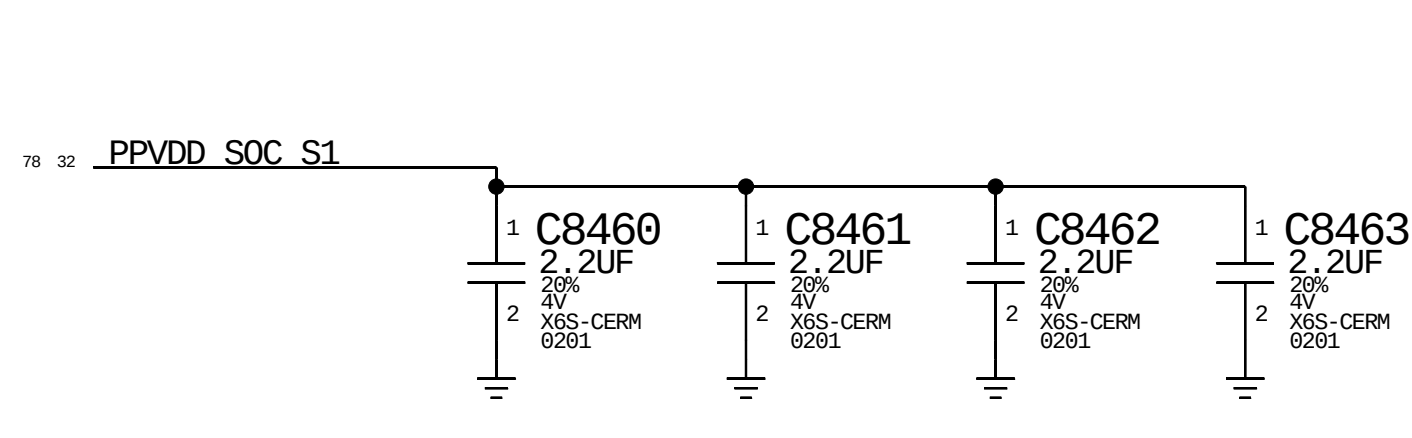
A BUCK 14 Filter



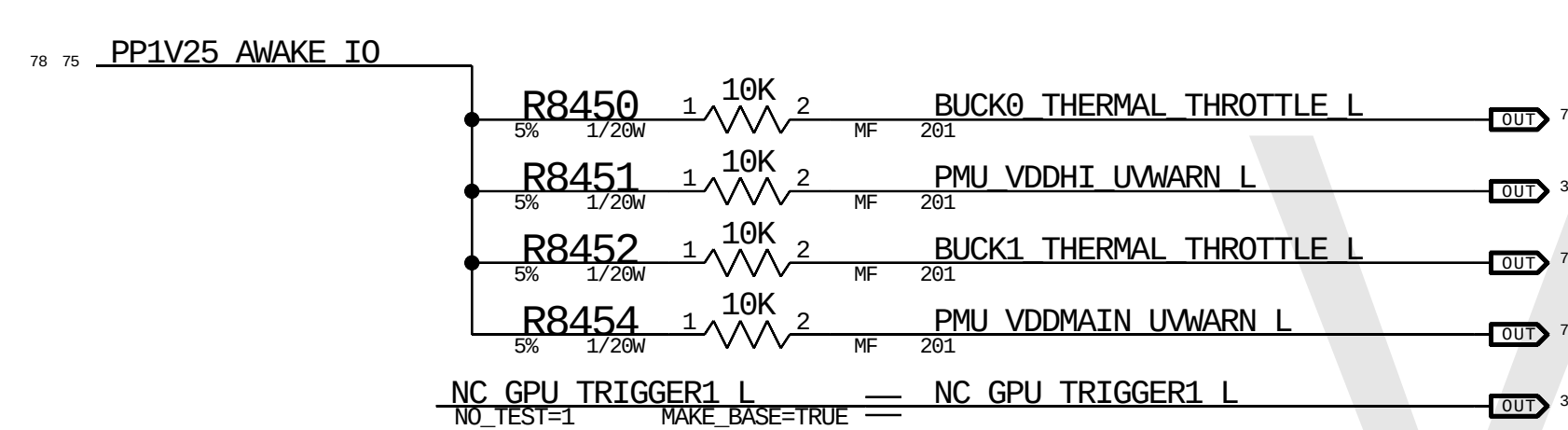
C PPVDD_PMU_LDO_PREREG Aliases



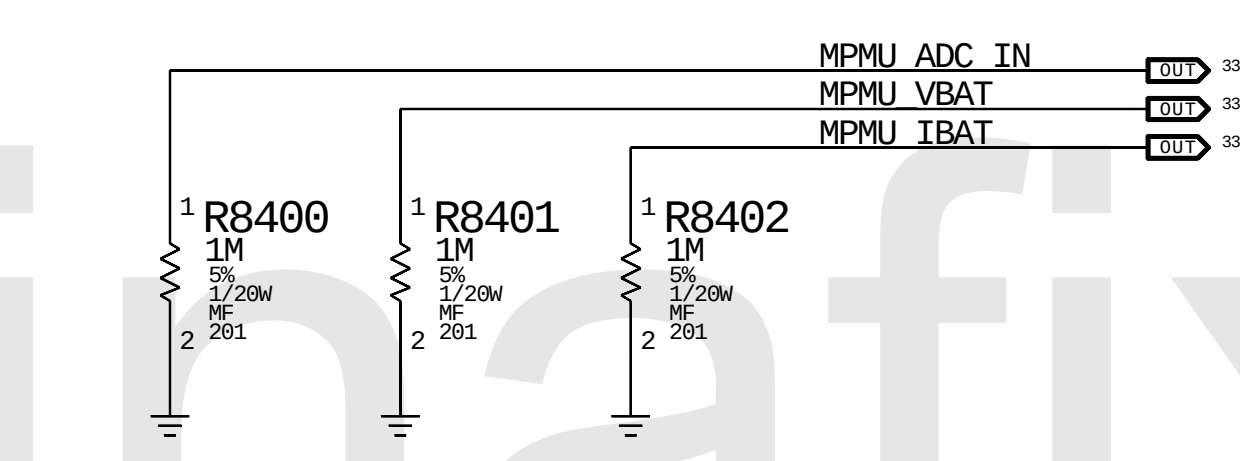
D PPVDD_SOC_S1 Decoupling



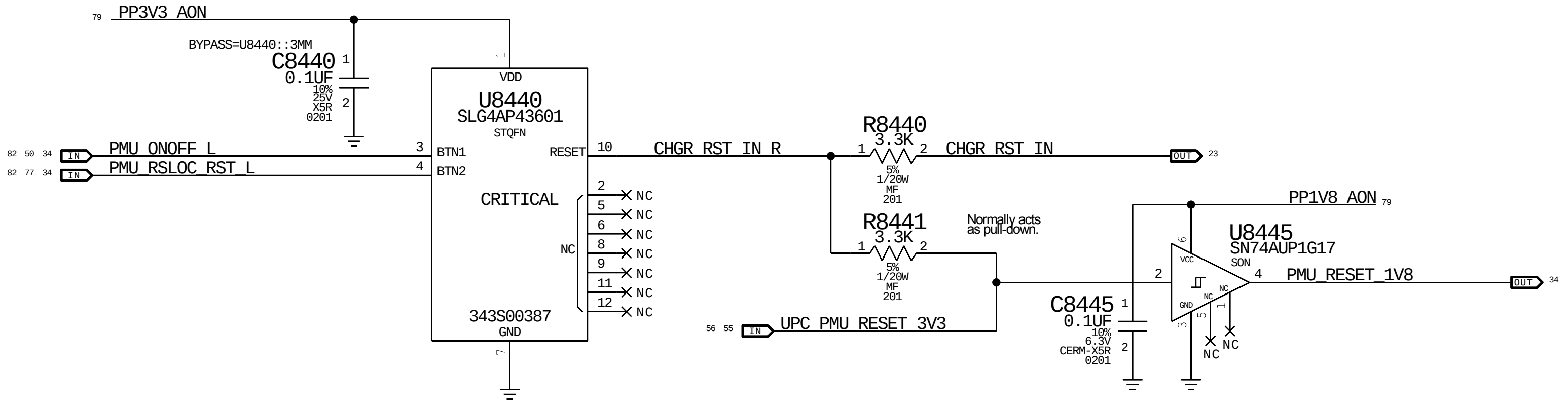
E PMU Control Flag Pull-Ups



F PMU Input Protection



I PMU_RESET_1V8 Generation

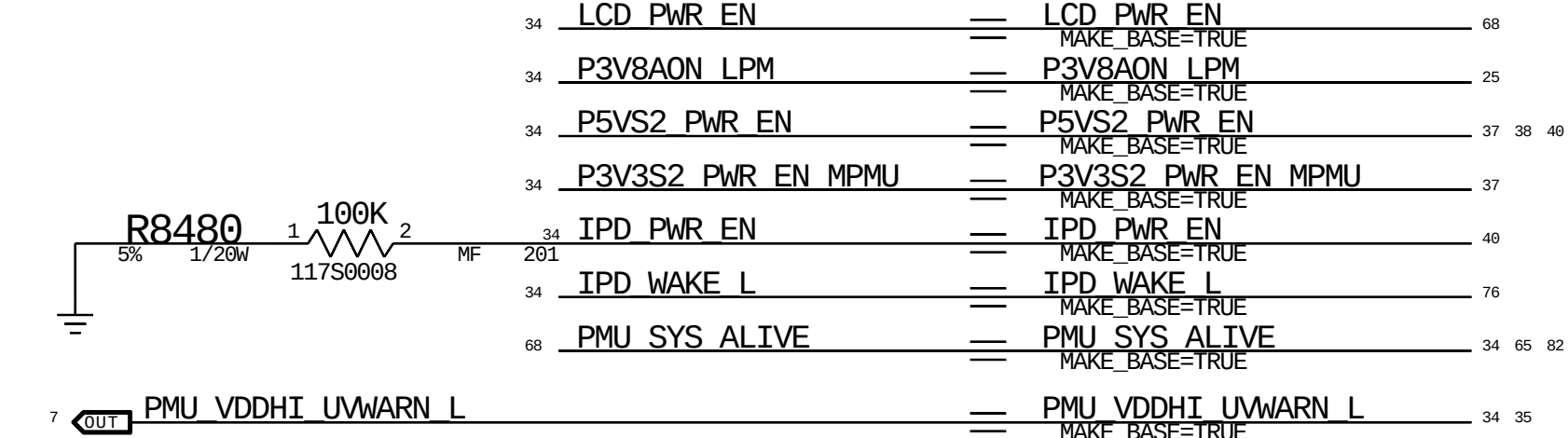


J PMU NC Aliases

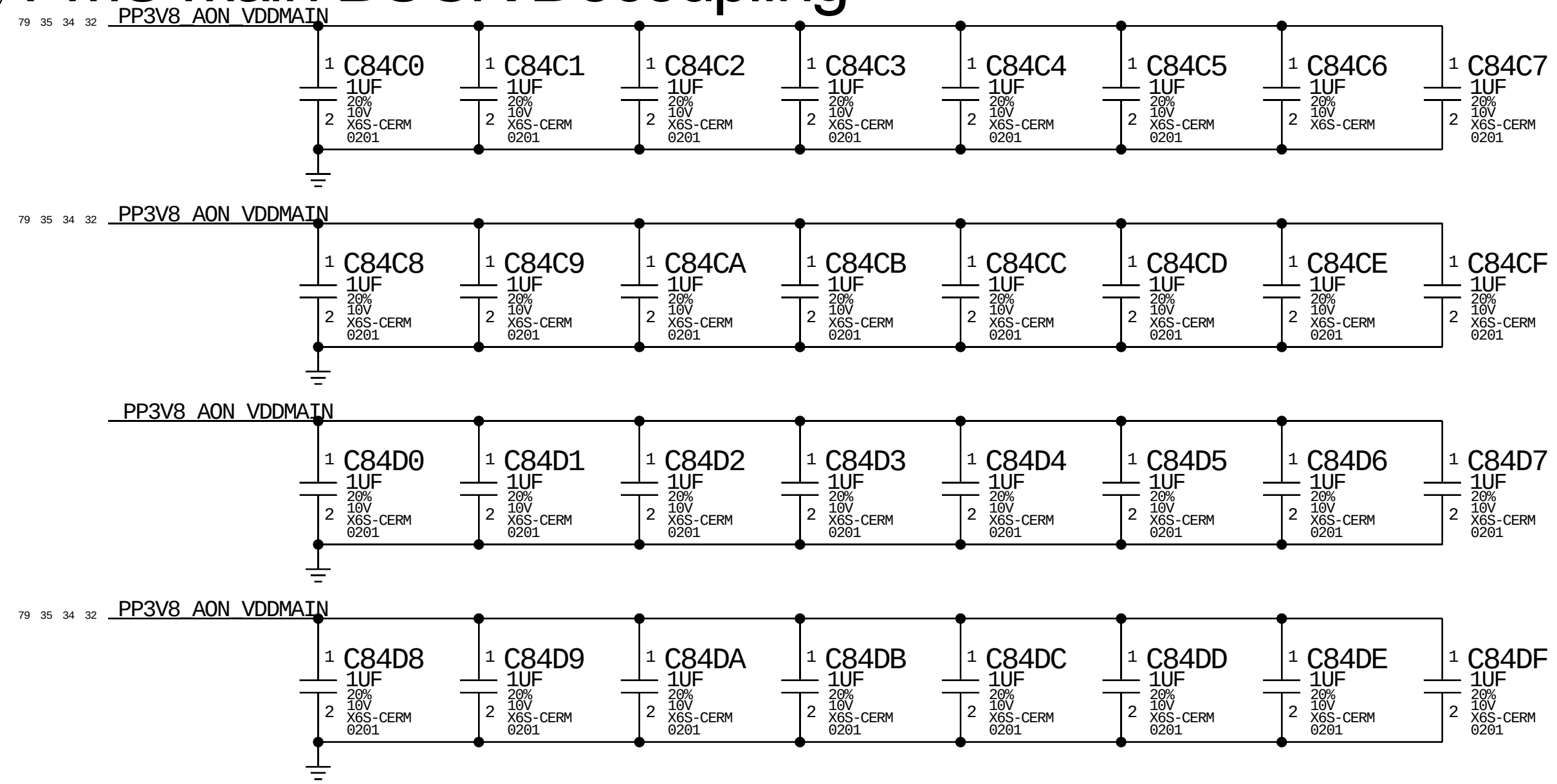
NC HDMI CEC IRQ	==	NC HDMI CEC IRQ
NC USB3 WAKE	==	NC USB3 WAKE
NC HDMI RESET_L	==	NC HDMI RESET_L
NC USB3 PWR_EN	==	NC USB3 PWR_EN
NC MPMU GPIO24	==	NC MPMU GPIO24
NC MPMU LDO1_EN	==	NC MPMU LDO1_EN
NC_FAN_PWR_EN	==	NC_FAN_PWR_EN
NC_MPMU_GPIO27	==	NC_MPMU_GPIO27

NC_MPMU_VLD05	==	NC_MPMU_VLD05
NC_MPMU_VLD010	==	NC_MPMU_VLD010
NC_MPMU_VLD013	==	NC_MPMU_VLD013
NC_MPMU_VLD014	==	NC_MPMU_VLD014
NC_MPMU_VLD016	==	NC_MPMU_VLD016
NC_MPMU_BUTTON3	==	NC_MPMU_BUTTON3
NC_MPMU_BUTTON4	==	NC_MPMU_BUTTON4
NC_MPMU_BUTTON01	==	NC_MPMU_BUTTON01
NC_MPMU_BUTTON02	==	NC_MPMU_BUTTON02
NC_MPMU_BUTTON03	==	NC_MPMU_BUTTON03

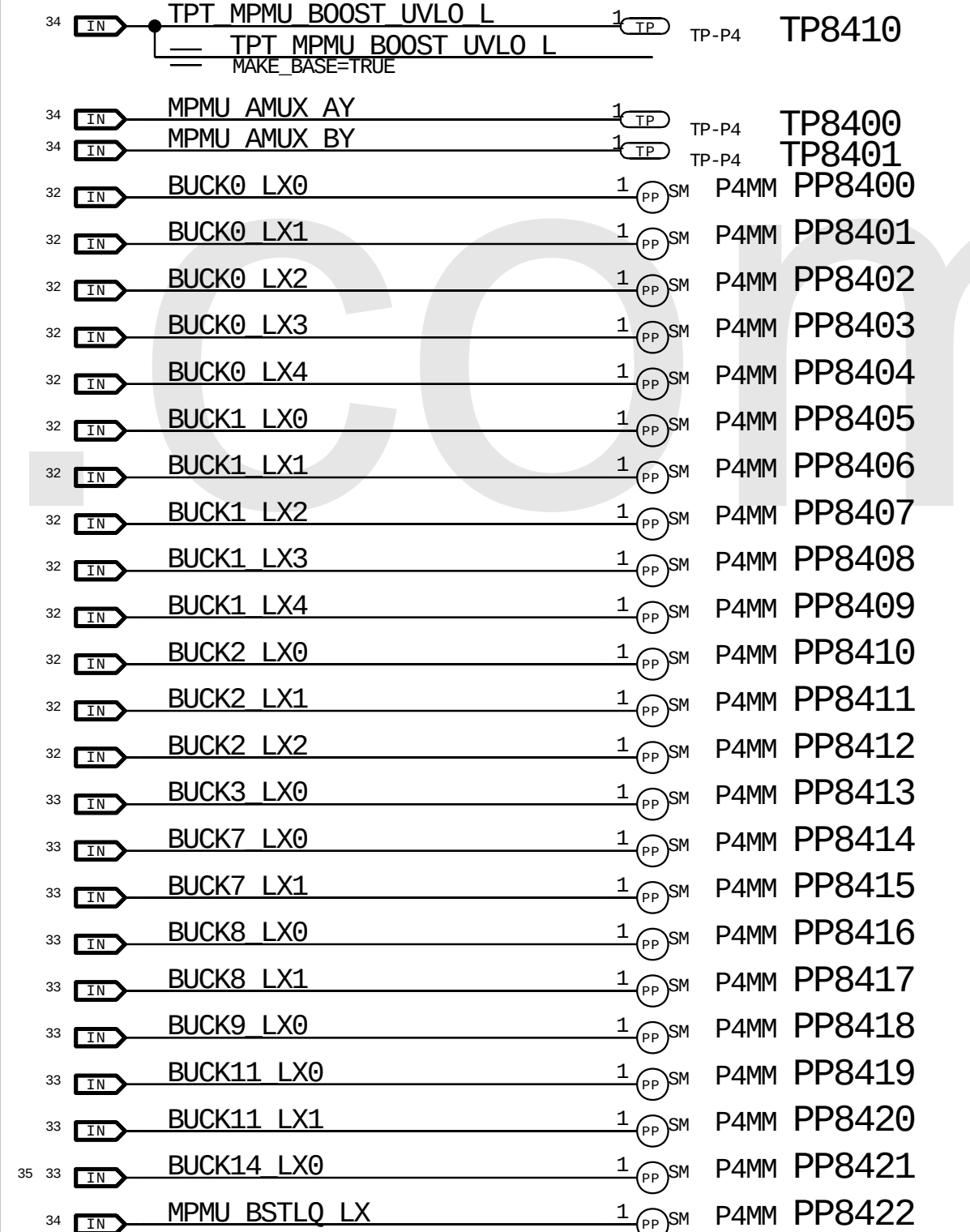
K PMU Signal Aliases



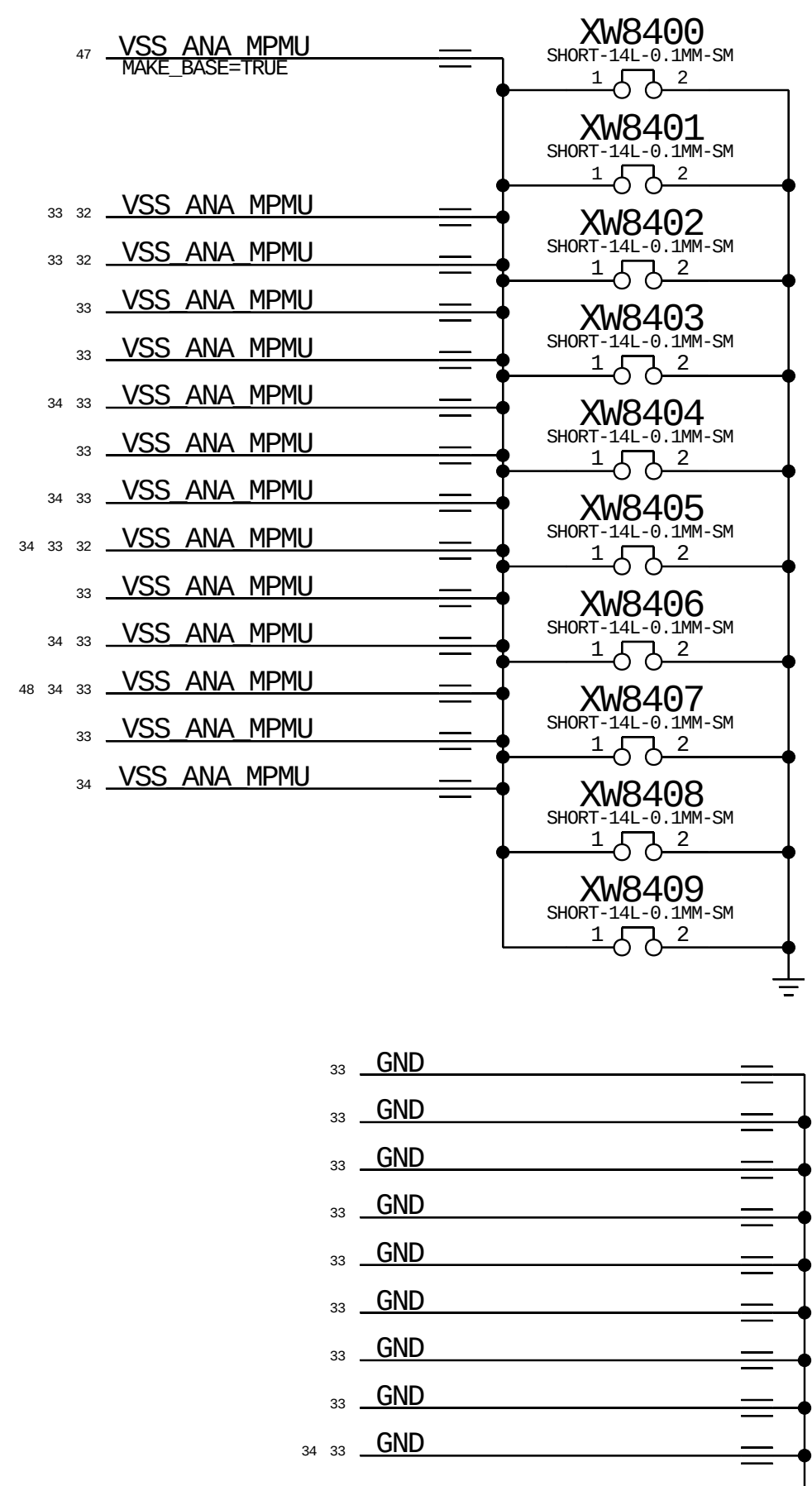
B PMU Main BUCK Decoupling



G PMU Test Points

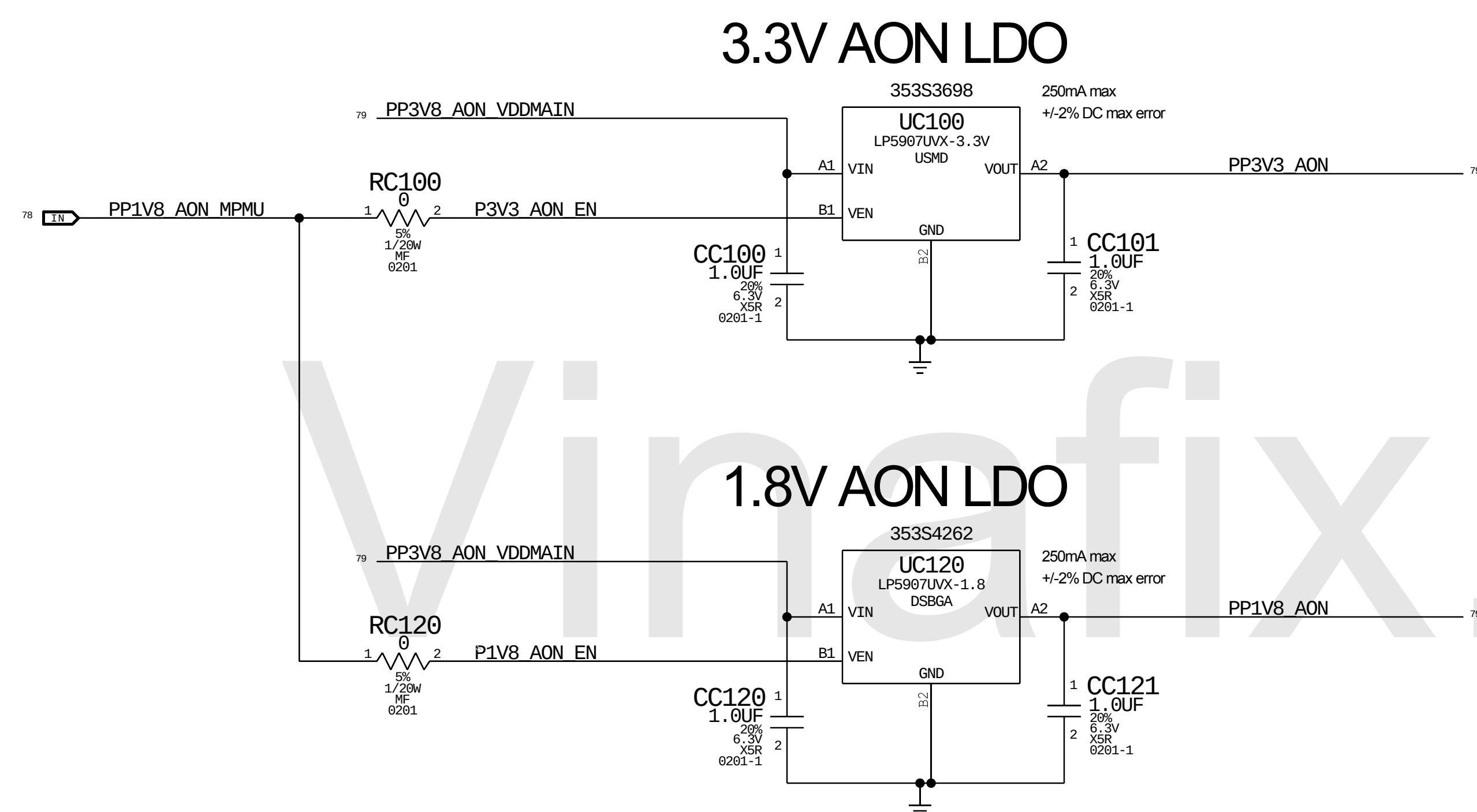


H PMU GND Aliases

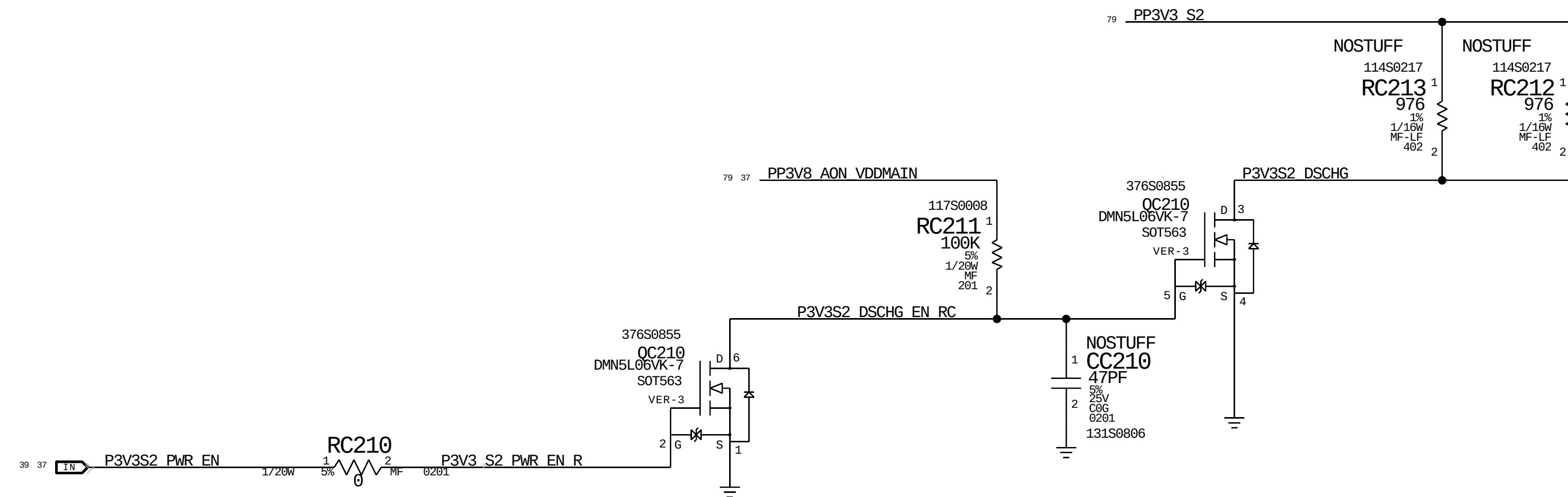


PMU: Master extra

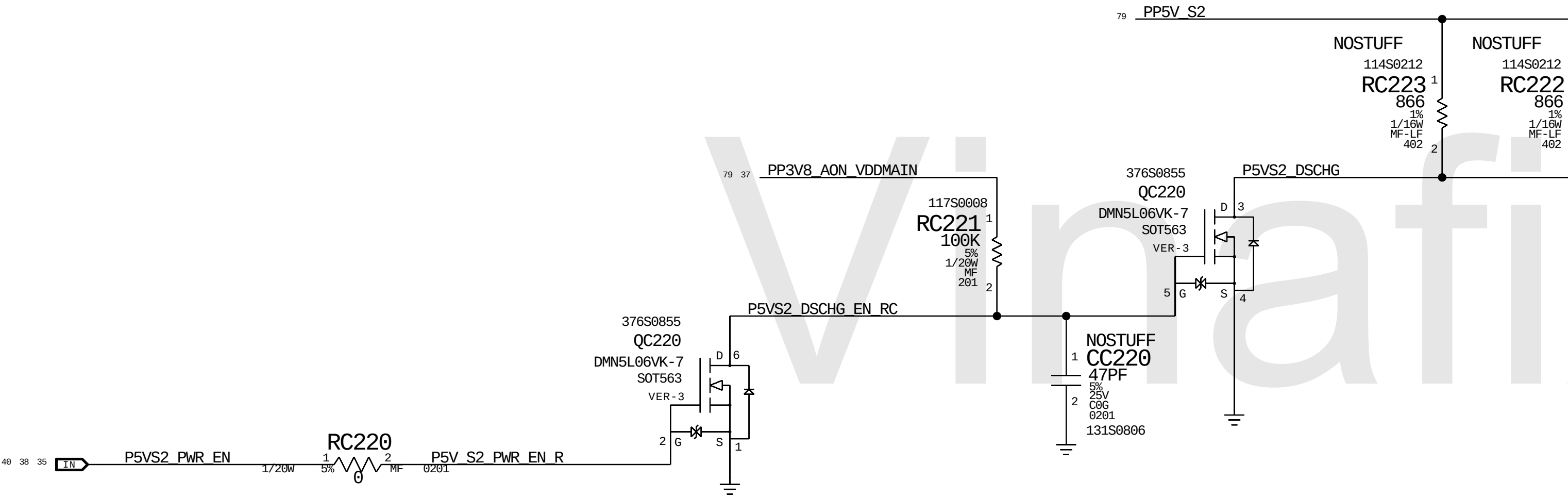
BOM_COST_GROUP=PLATFORM POWER



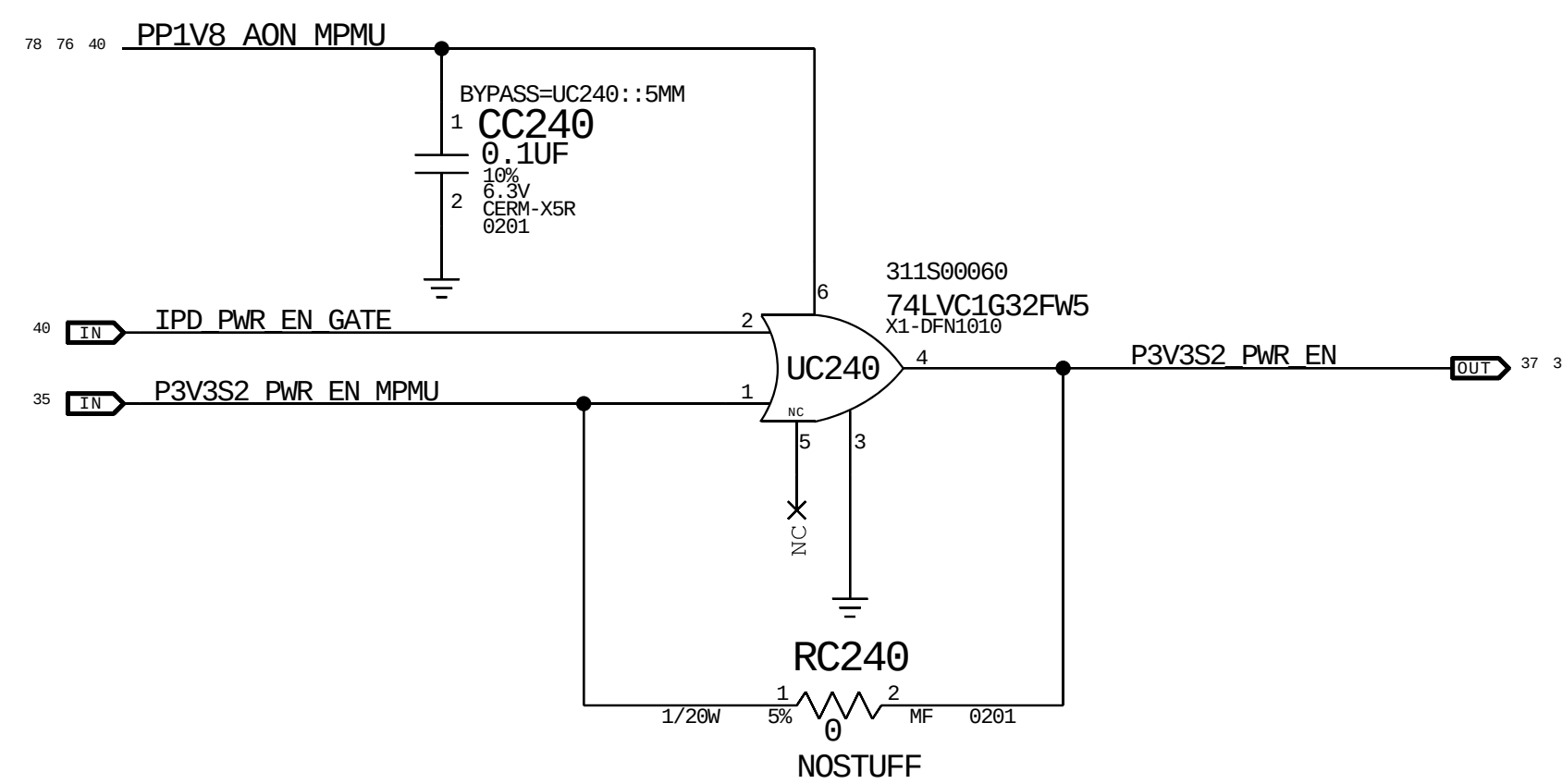
A PP3V3_S2 Discharge Circuit



B PP5V_S2 Discharge Circuit



C P3V3S2_PWR_EN Gating Logic



NOTE:
Per Sera PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.
IPD_PWR_EN and PP5V_S2_EN were moved to GPIOs that Sera PMU can "hold" off.

D PP3V3_S2 Probe Points

PPC200	P3V3S2_EN	PPC203	P3V3S2_V0S
PPC201	P3V3S2_PG00D	PPC204	P3V3S2_SW
PPC202	P3V3S2_FB_LPF		

E PP5V_S2 Probe Points

PPC210	P5VS2_EN	PPC213	P5VS2_FB_RC
PPC211	P5VS2_PG00D	PPC214	P5VS2_SW
PPC212	P5VS2_FB_XW	PPC215	GND

POWER: 5V, 3V3 Support

* OK2INTEGRATE *

5V_S2 Voltage Regulator

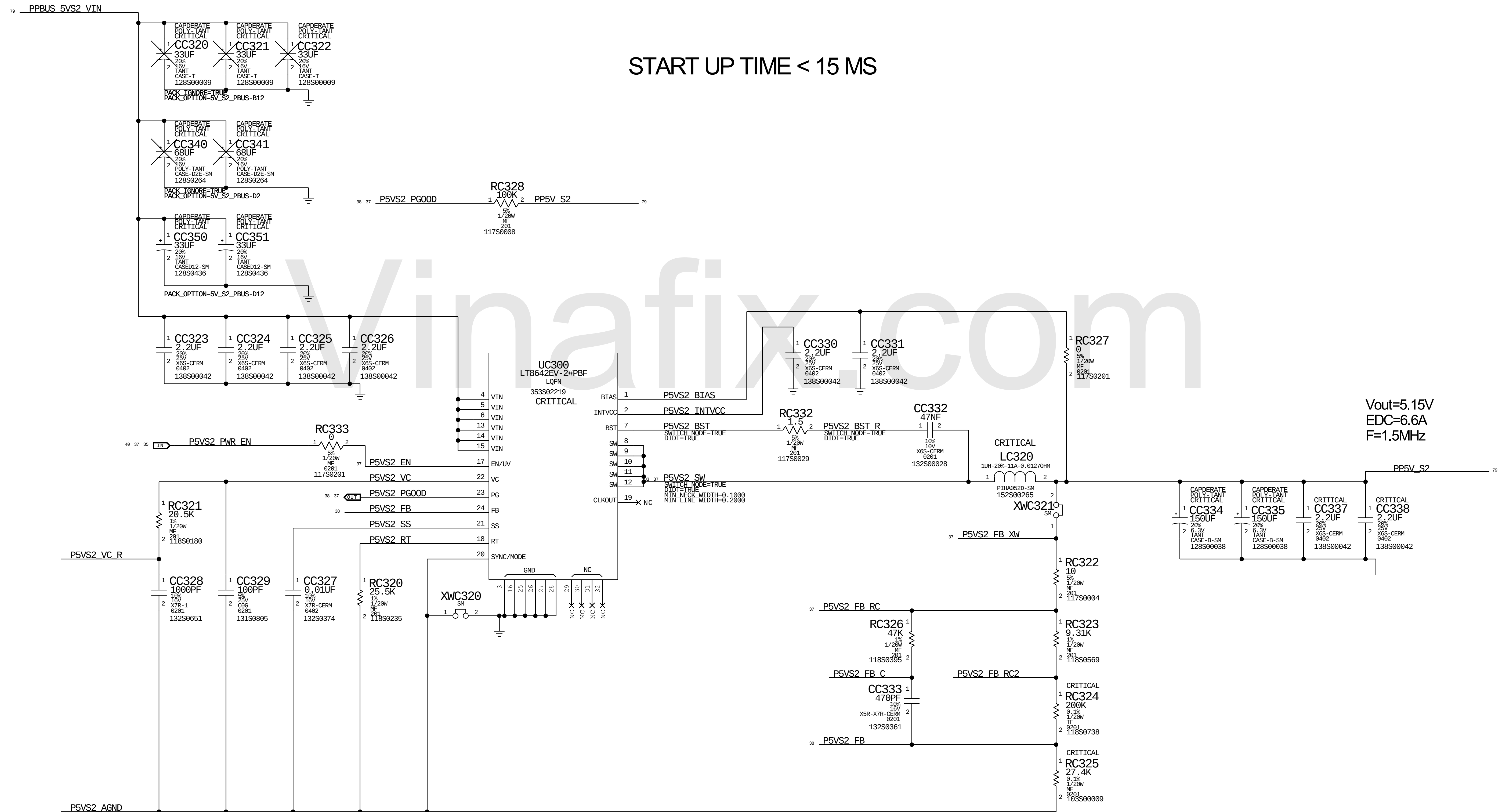
SET ONE OPTION FOR PBUS CAPS

PACK OPTION=5V S2 PBUS-B12

PACK_OPTION=5V_S2_PBUS-D2

PACK_OPTION=5V_S2_PBUS-D12

START UP TIME < 15 MS



POWER: 5V S2

BOM_COST_GROUP=PLATFORM POWER

*** OK2INTEGRATE ***

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

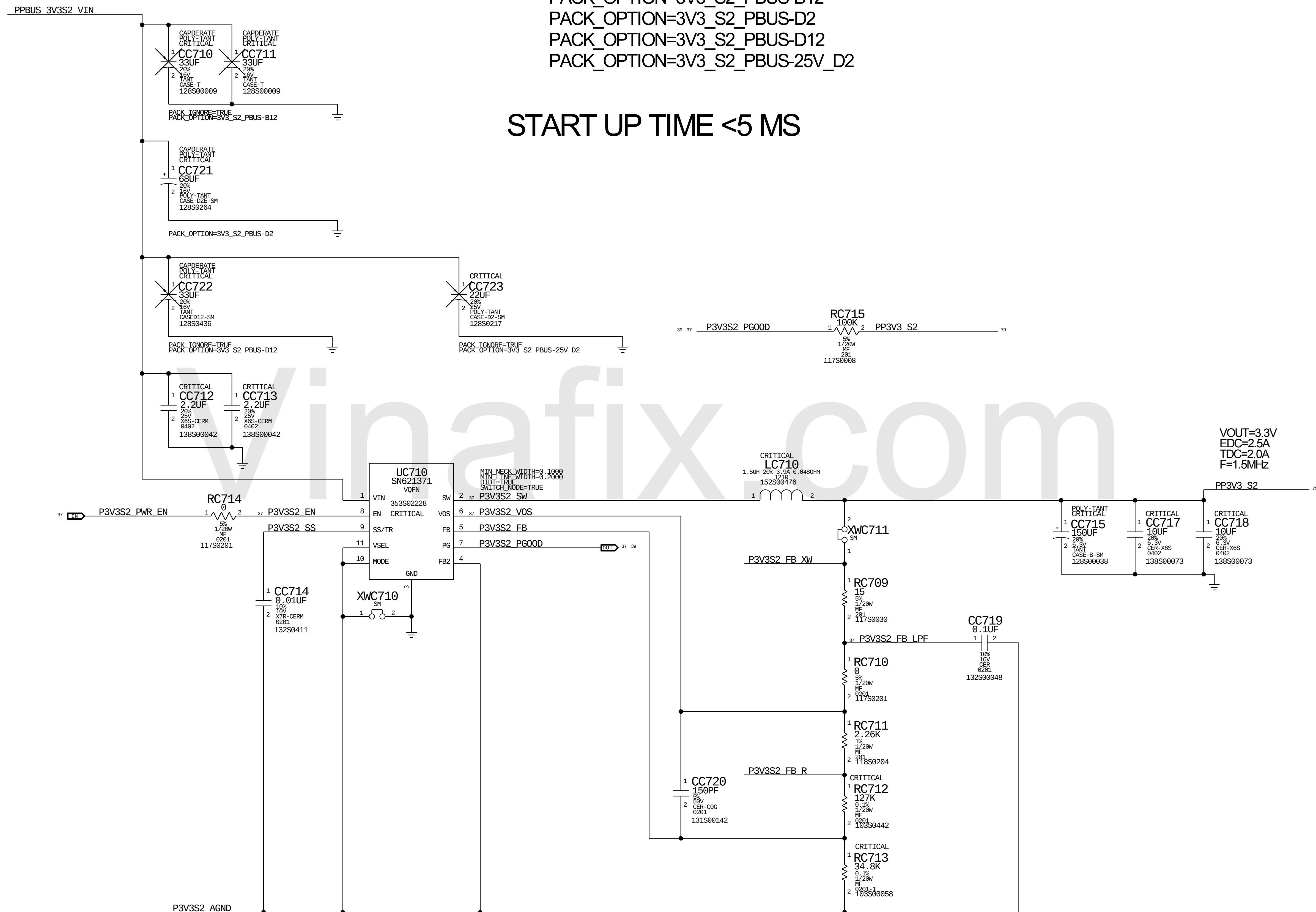
PACK_OPTION=3V3_S2_PBUS-B12

PACK_OPTION=3V3_S2_PBUS-D2

PACK_OPTION=3V3_S2_PBUS-D12

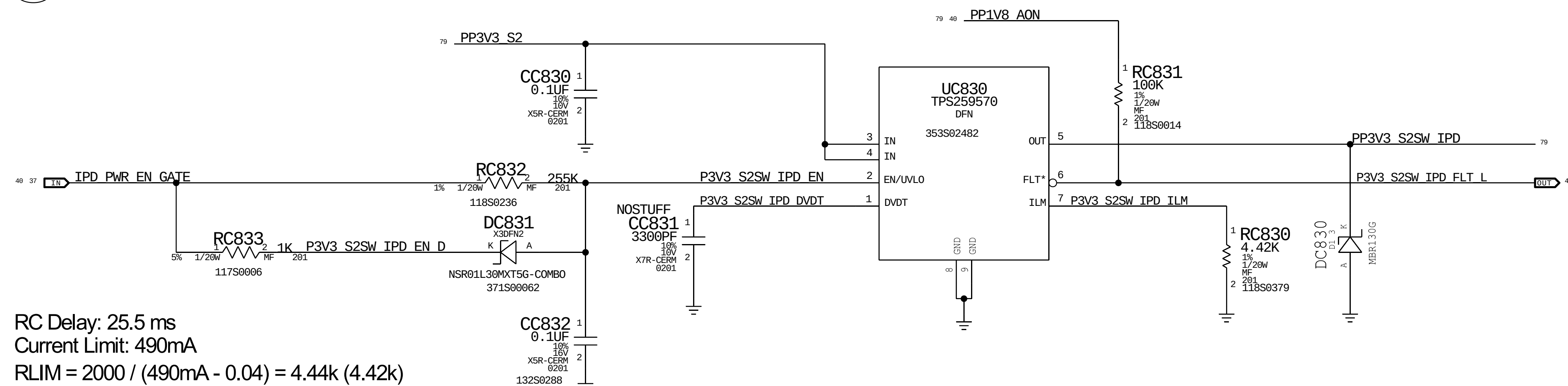
PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS



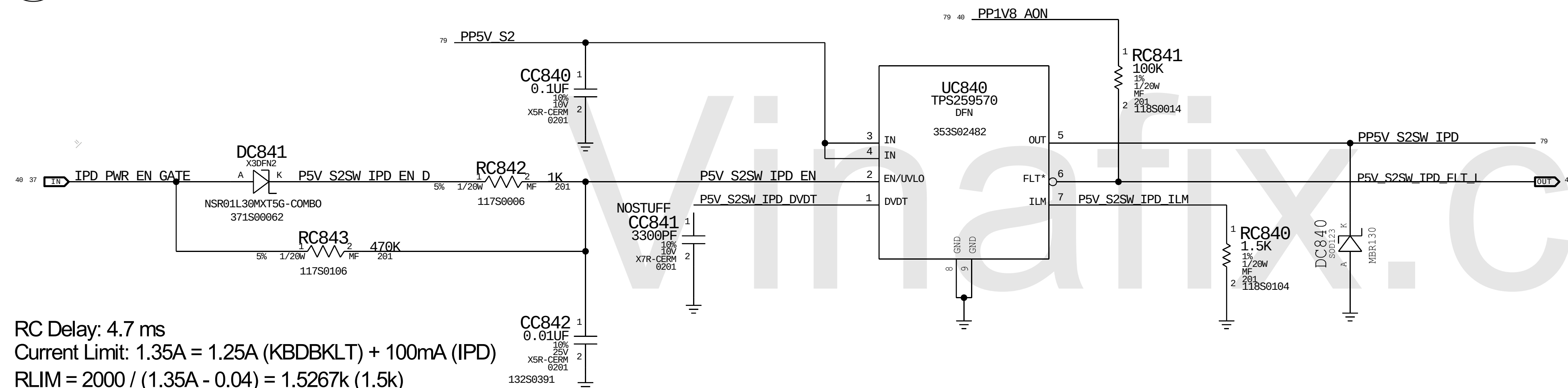
POWER: 3V3 S2

A PP3V3_S2SW_IPD Load Switch & e-Fuse



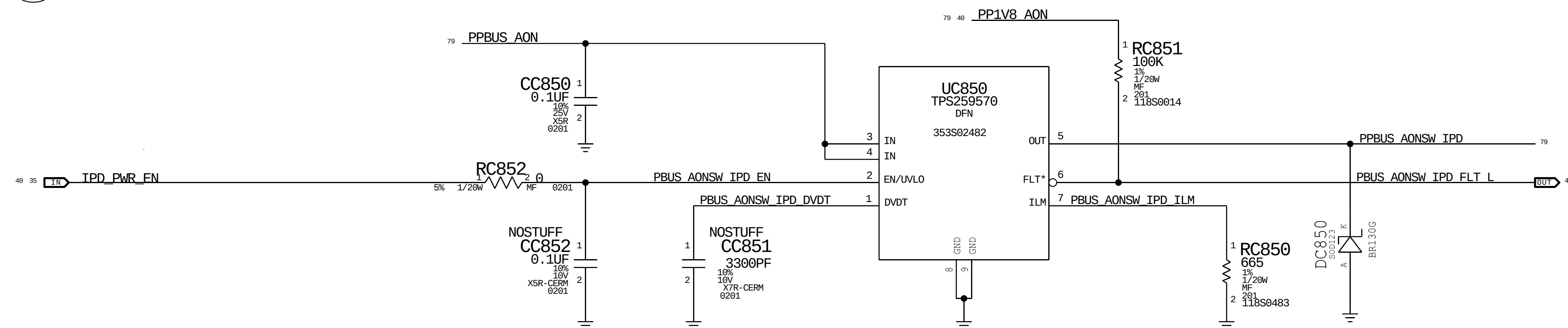
RC Delay: 25.5 ms
Current Limit: 490mA
 $RLIM = 2000 / (490mA - 0.04) = 4.44k$ (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

B PP5V_S2SW_IPD Load Switch & e-Fuse



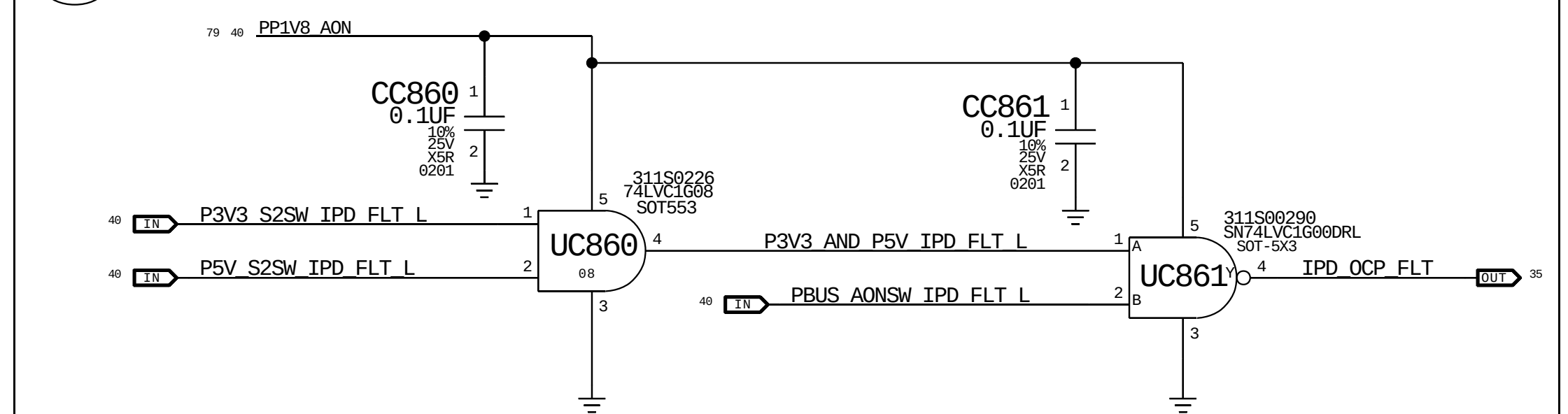
RC Delay: 4.7 ms
Current Limit: $1.35A = 1.25A$ (KBDBKLT) + 100mA (IPD)
 $RLIM = 2000 / (1.35A - 0.04) = 1.5267k$ (1.5k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

C PPBUS_AONSW_IPD Load Switch & e-Fuse

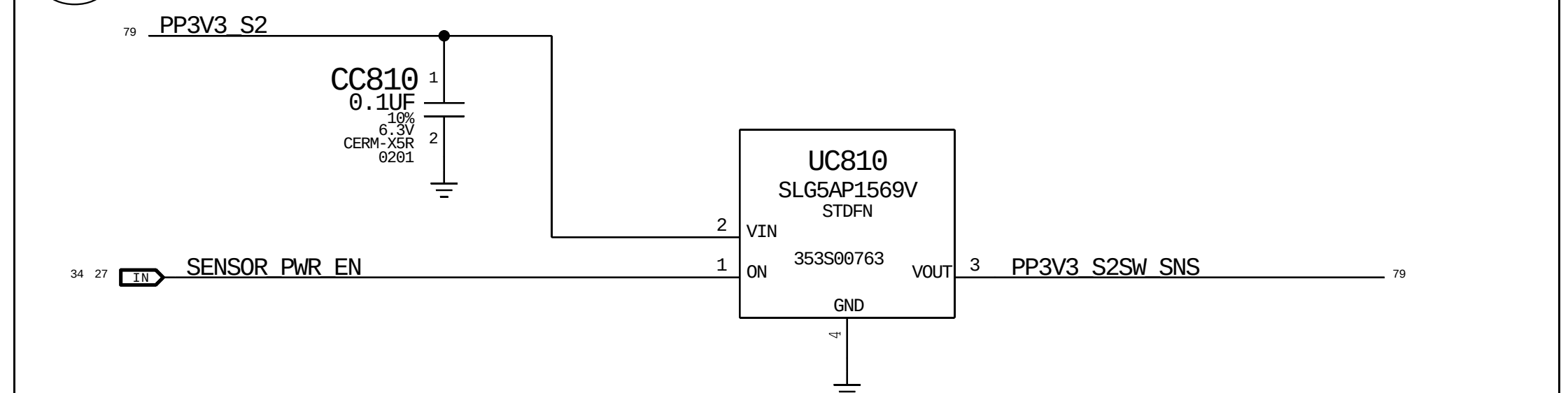


Current Limit: 3A
 $RLIM = 2000 / (3A - 0.04) = 676$ (665)
/FLT Open Drain
Self-Controlled (EN = 3.13V to 5.93V)

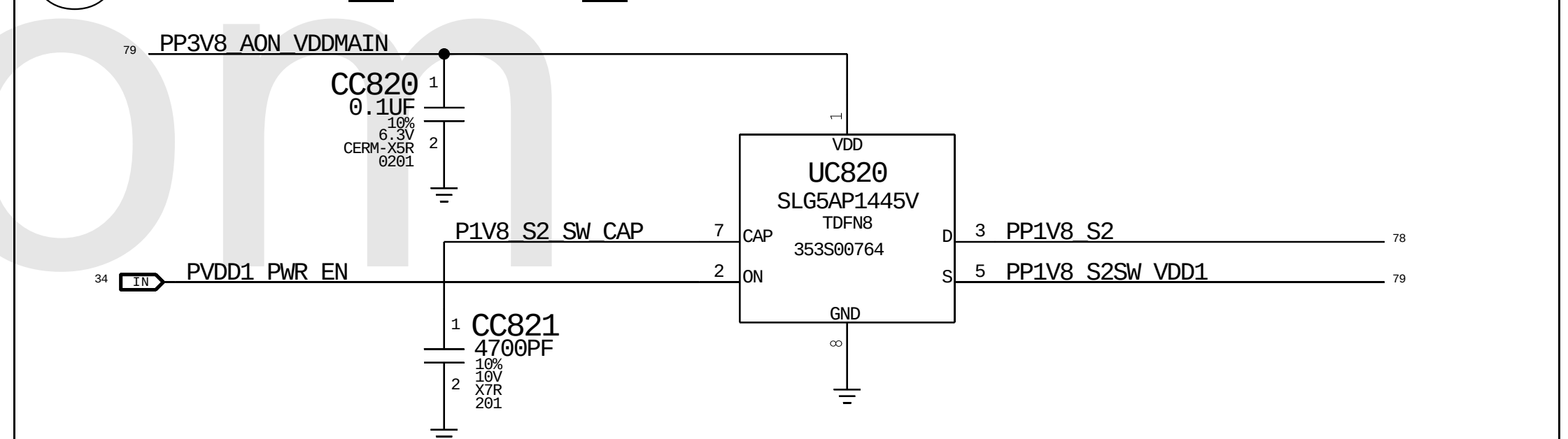
D IPD OCP Fault



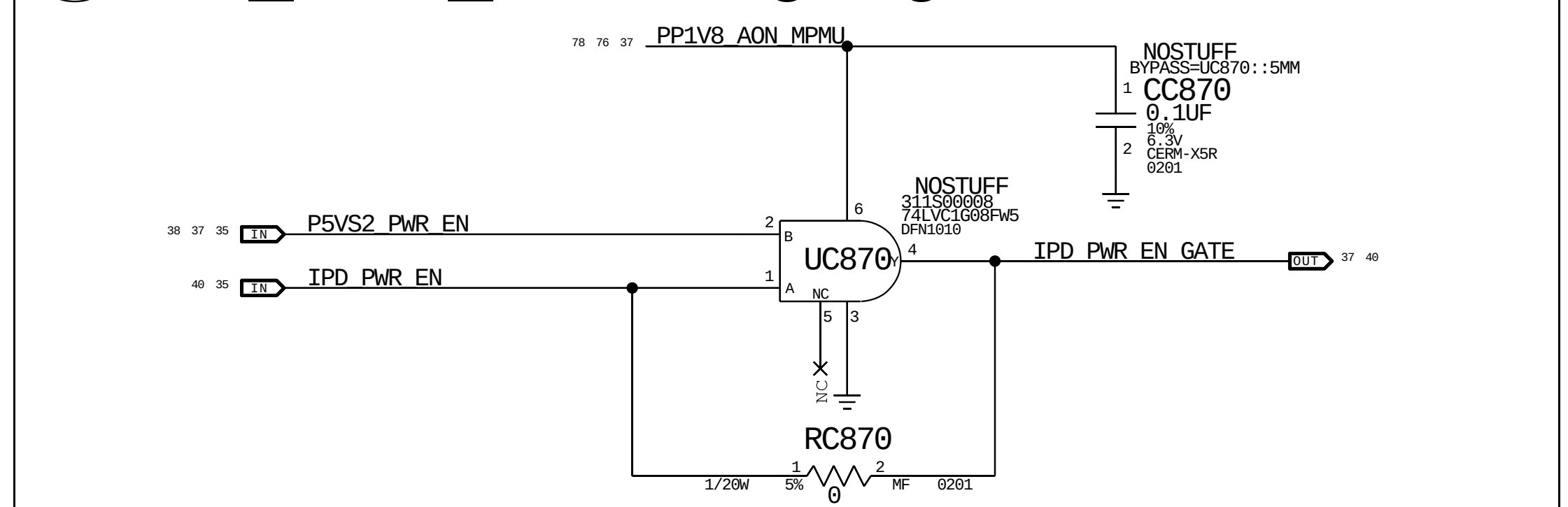
E PP3V3_S2SW_SNS Load Switch



F PP1V8_S2SW_VDD1 Load Switch



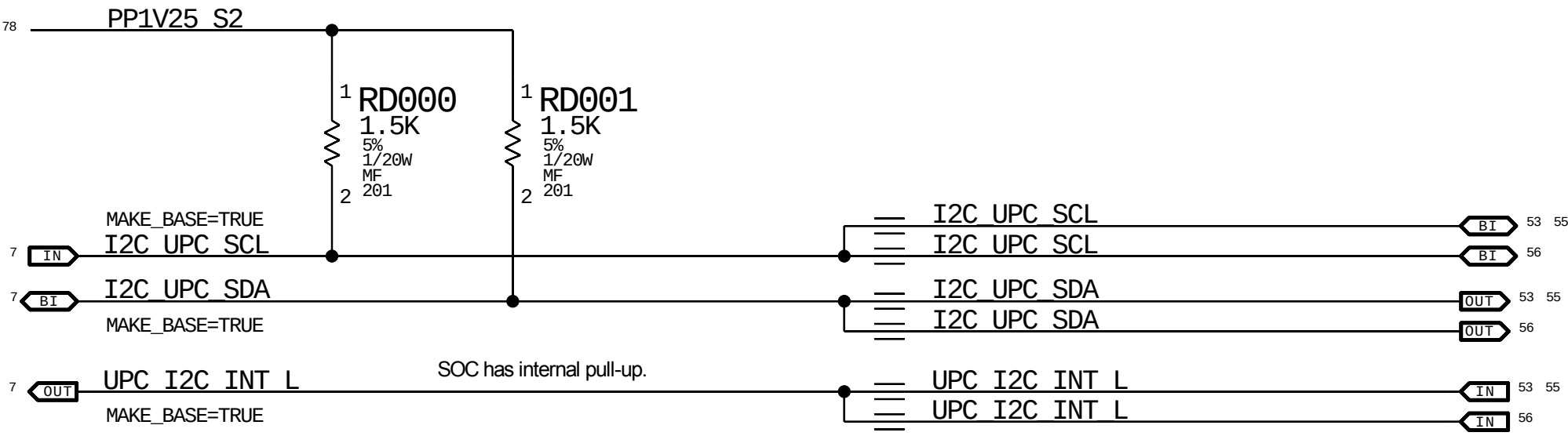
G IPD_PWR_EN Gating Logic



Power: Load Switches

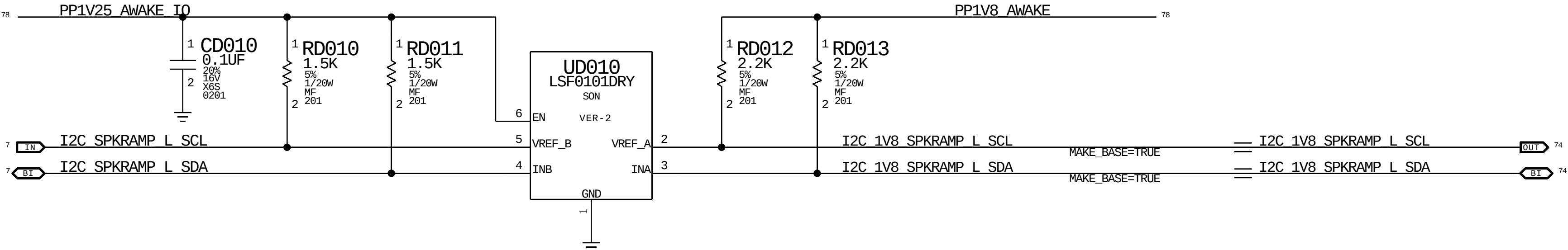
SIO I2C0

DEVICE	DEV	WR	RD
ACE 0	0x38	0x70	0x71
ACE 1	0x3F	0x7E	0x7F



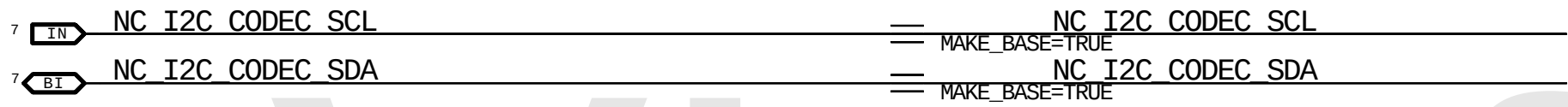
SIO I2C1

DEVICE	DEV	WR	RD
SPKRAMP L	0x31	0x62	0x63



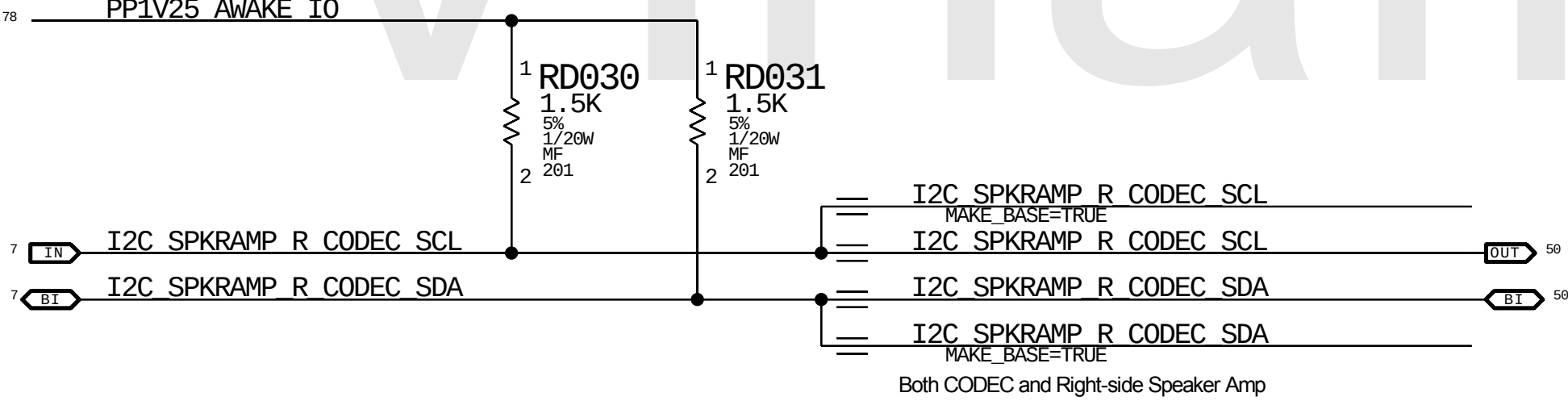
SIO I2C2

DEVICE	DEV	WR	RD
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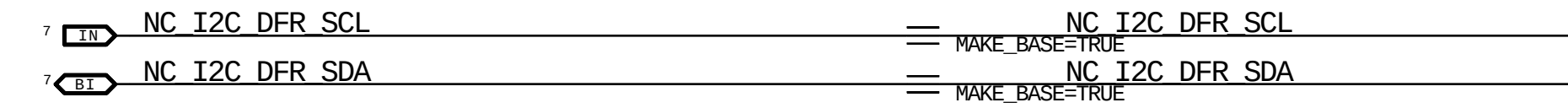
SIO I2C3

DEVICE	DEV	WR	RD
SPKRAMP R	0x34	0x68	0x69
CODEC	0x48	0x90	0x91



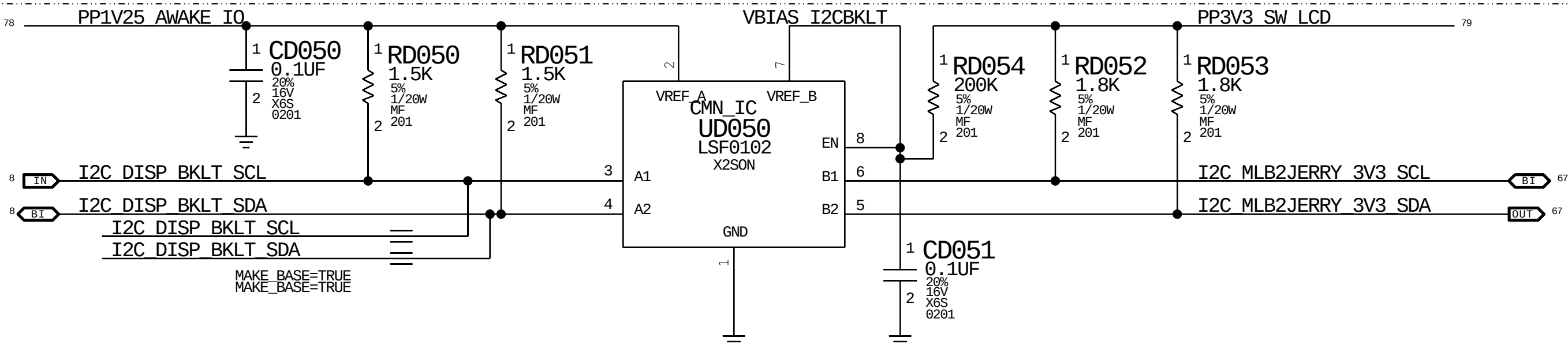
SIO I2C4

DEVICE	DEV	WR	RD
--------	-----	----	----



DISP I2C

DEVICE	DEV	WR	RD
LP8549	0x2C	0x58	0x59



I2C: SIO, DISP

BOM_COST_GROUP=SMC

ISP I2C0

DEVICE	DEV	WR	RD
--------	-----	----	----

UNUSED

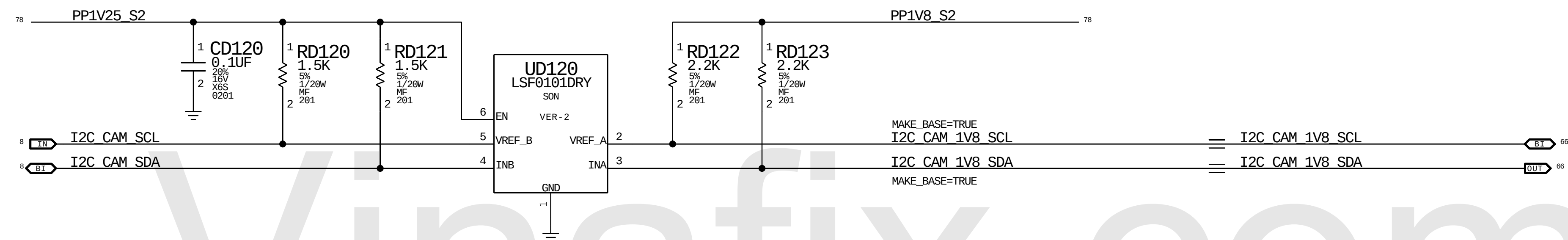
ISP I2C1

DEVICE	DEV	WR	RD
--------	-----	----	----

UNUSED

ISP I2C2

<u>DEVICE</u>	<u>DEV</u>	<u>WR</u>	<u>RD</u>
CAMERA	0x10	0x20	0x21
IMAGE SENSOR		0x36	0x6C 0x6D



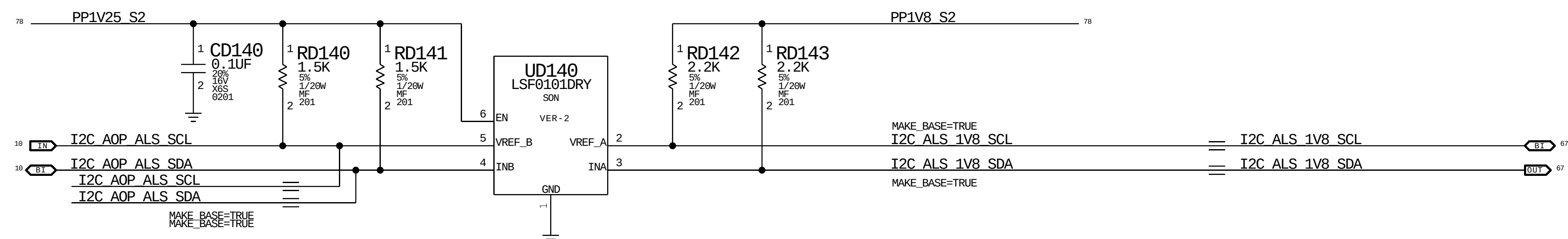
ISP I2C3

DEVICE	DEV	WR	RD
--------	-----	----	----

UNUSED

AOP I2C0

DEVICE	DEV	WR	RD
ALS	0x29	0x52	0x53



AOP I2C1

DEVICE	DEV	WR	RD
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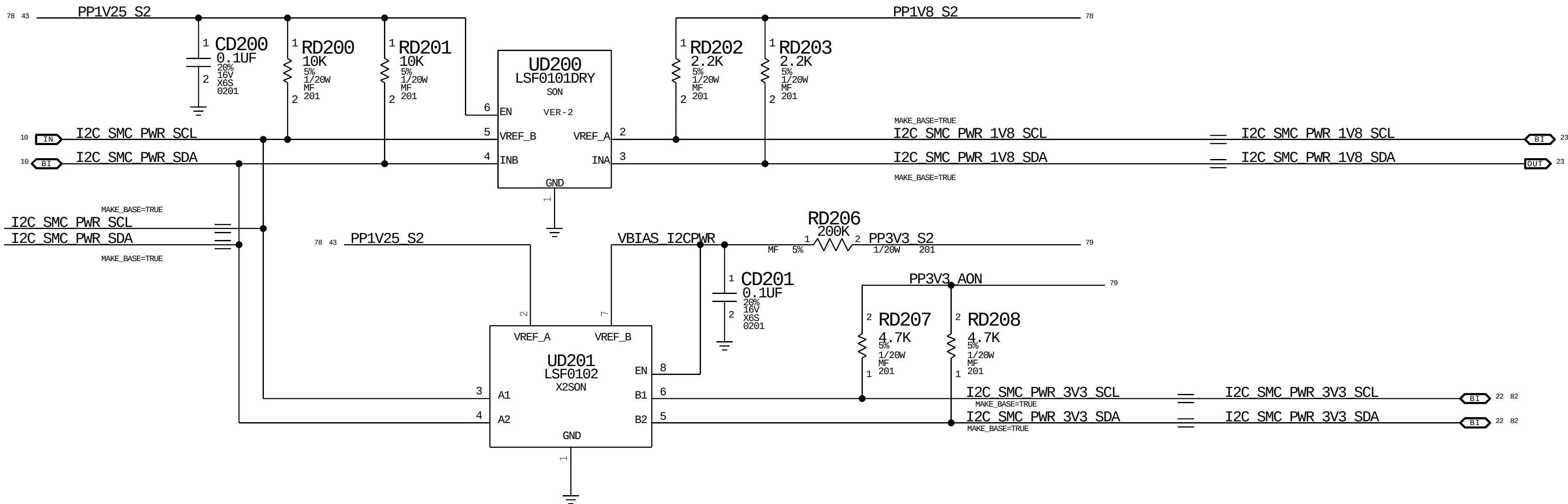
19	19	NC I2C AOP ENET SCL	NC I2C AOP ENET SCL
		MAKE_BASE=TRUE	NO_TEST=1
10	81	NC I2C AOP ENET SDA	NC I2C AOP ENET SDA
		MAKE_BASE=TRUE	NO_TEST=1

UNUSED

I2C: ISP, AOP	
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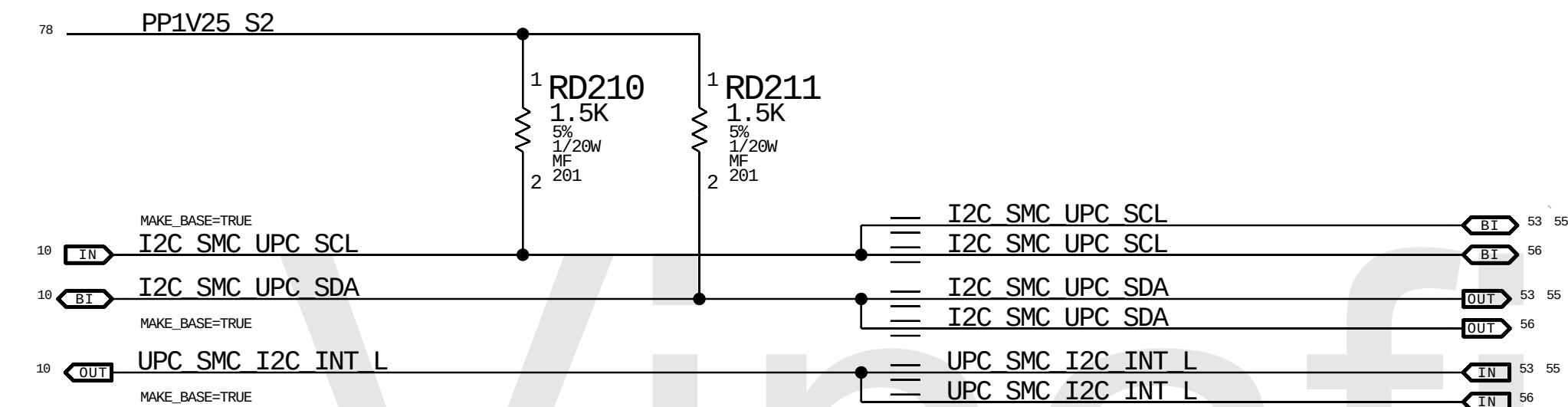
SMC I2C0

DEVICE DEV WR RD
CHARGER 0x00 0x12 0x13
BMU 0x0B 0x16 0x17



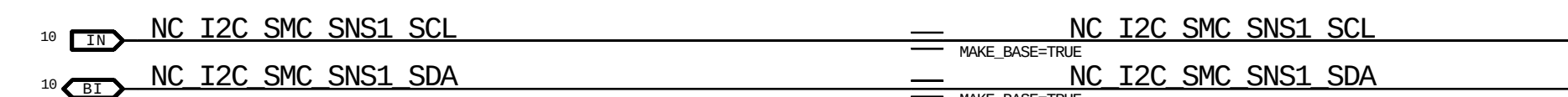
SMC I2C1

DEVICE DEV WR RD
ACE0 0x38 0x70 0x71
ACE1 0x3F 0x7E 0x7F



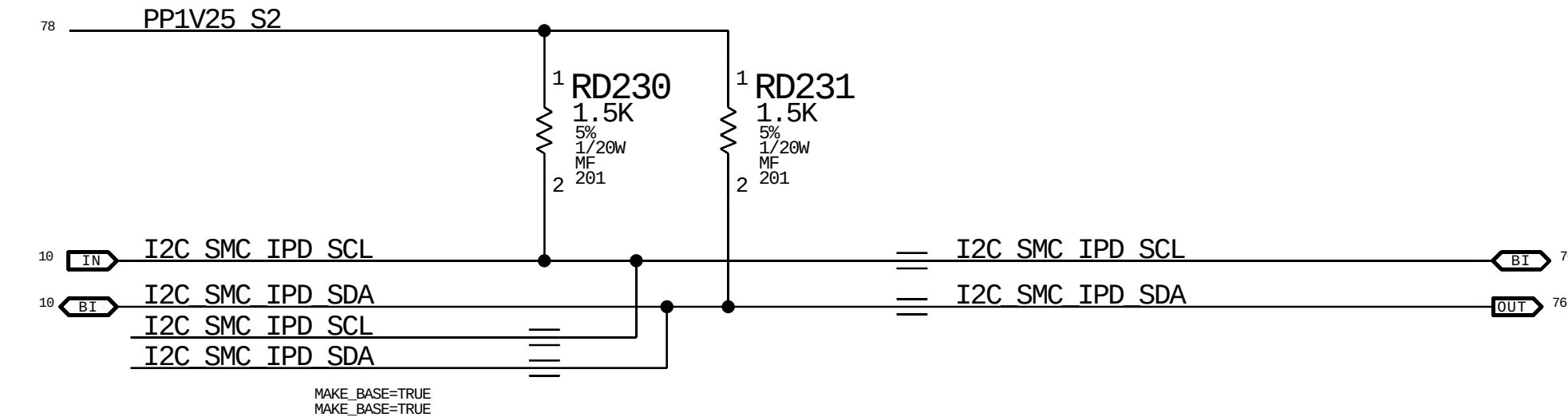
SMC I2C2

DEVICE DEV WR RD
TBD 0x- 0x- 0x-



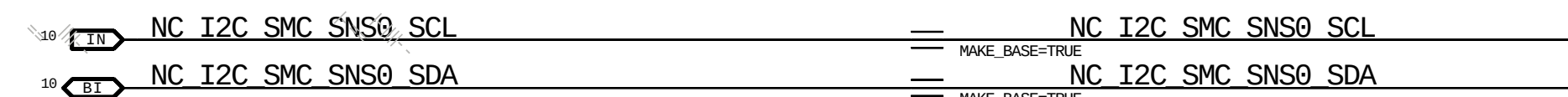
SMC I2C3

DEVICE DEV WR RD
PALMTEMP 0x4C 0x98 0x99



SMC I2C4

DEVICE DEV WR RD
TBD 0x- 0x- 0x-

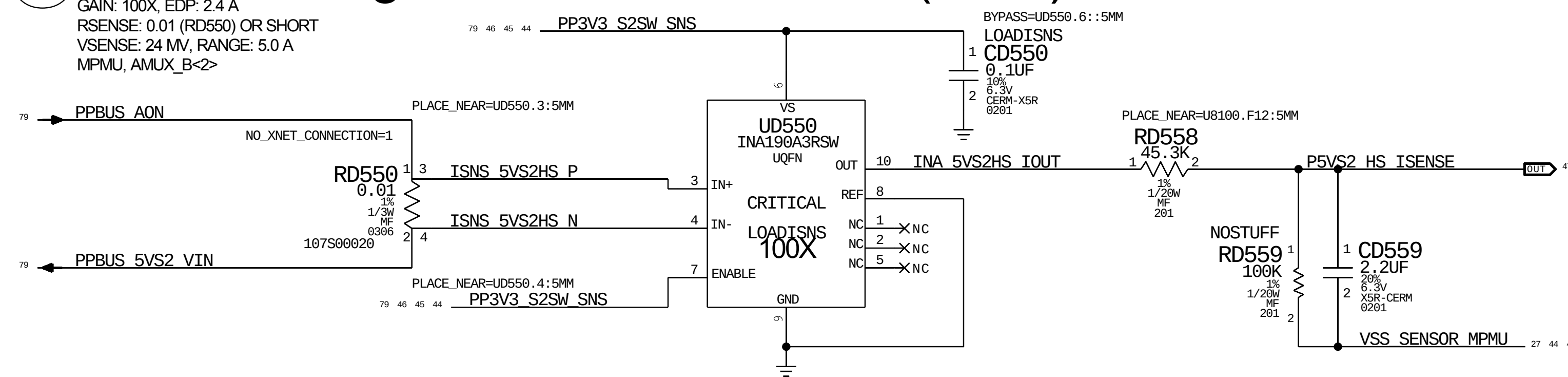


UNUSED

UNUSED

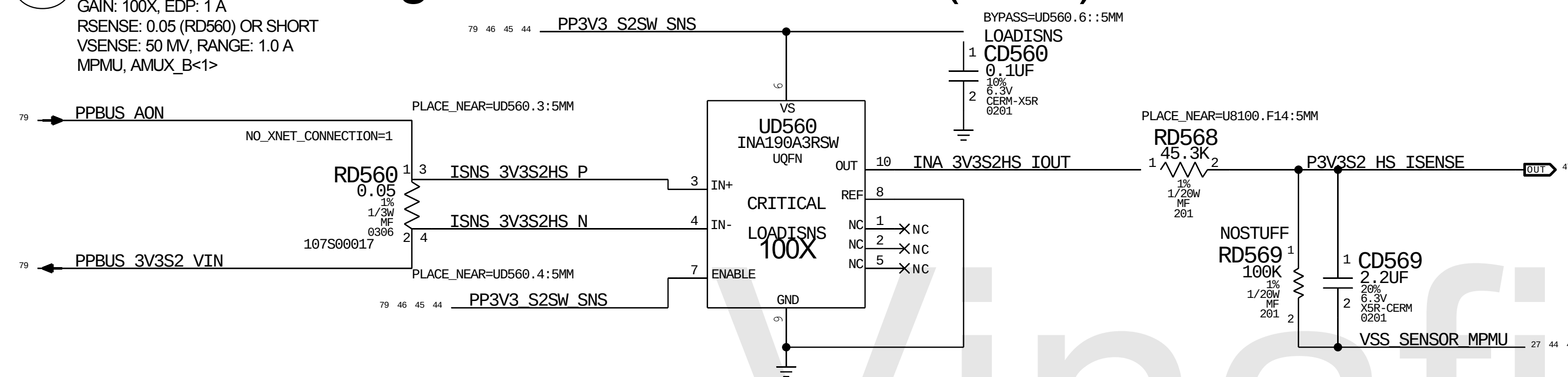
A 5V S2 VR High Side Current Sensor (IO5R)

GAIN: 100X, EDP: 2.4 A
RSENSE: 0.01 (RD550) OR SHORT
VSENSE: 24 mV, RANGE: 5.0 A
MPMU, AMUX_B<2>



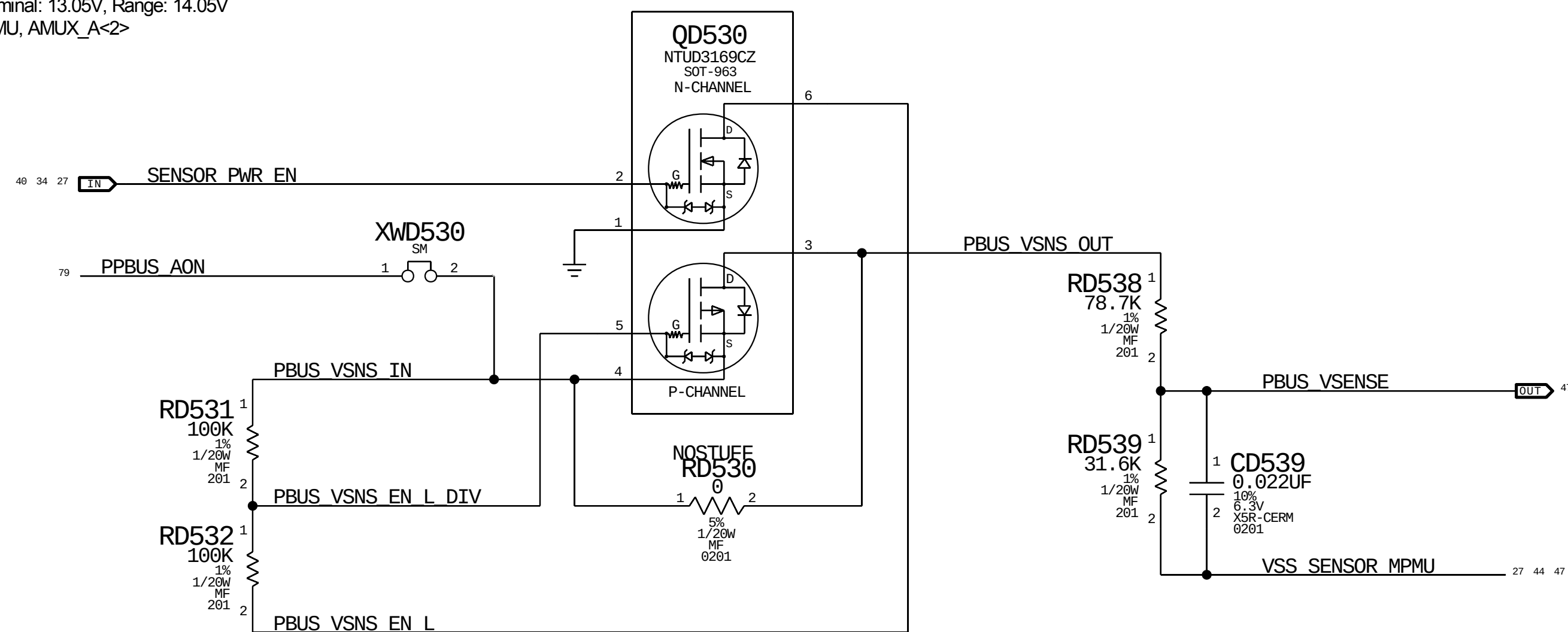
B 3V3 S2 VR High Side Current Sensor (IO3R)

GAIN: 100X, EDP: 1 A
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 50 mV, RANGE: 1.0 A
MPMU, AMUX_B<1>



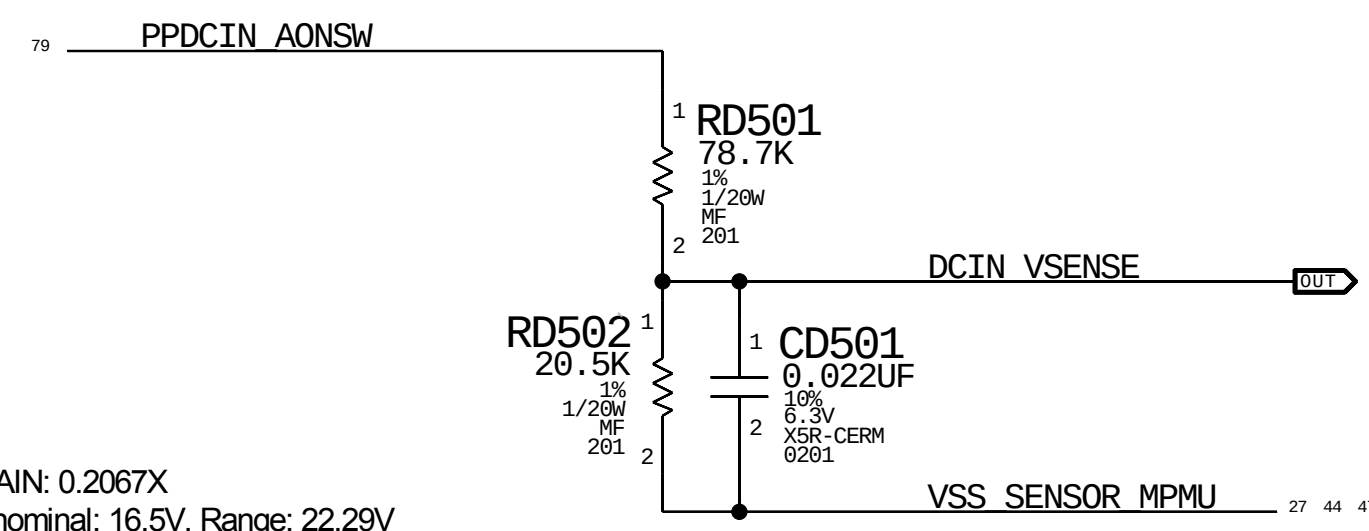
C PPBUS Voltage Sensor (VP0R)

GAIN: 0.2865X
Vnominal: 13.05V, Range: 14.05V
MPMU, AMUX_A<2>



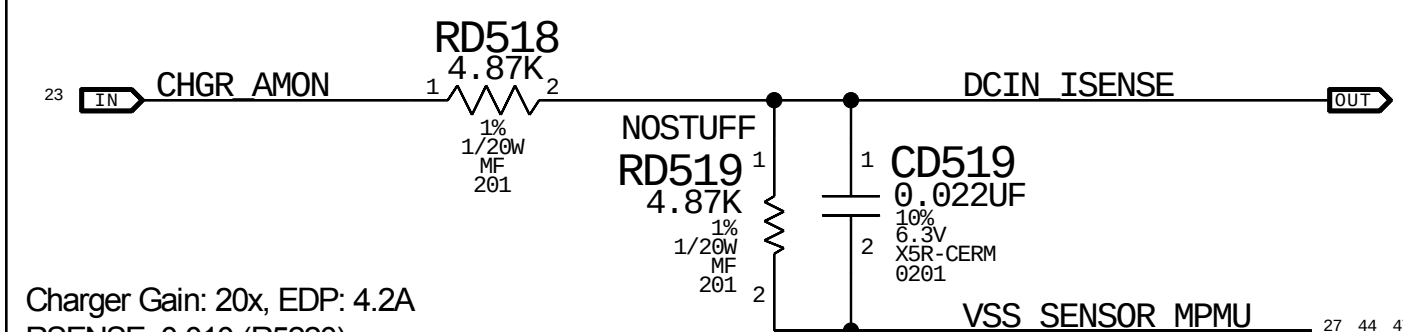
D DCIN Voltage Sensor (VD0R)

GAIN: 0.2067X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>



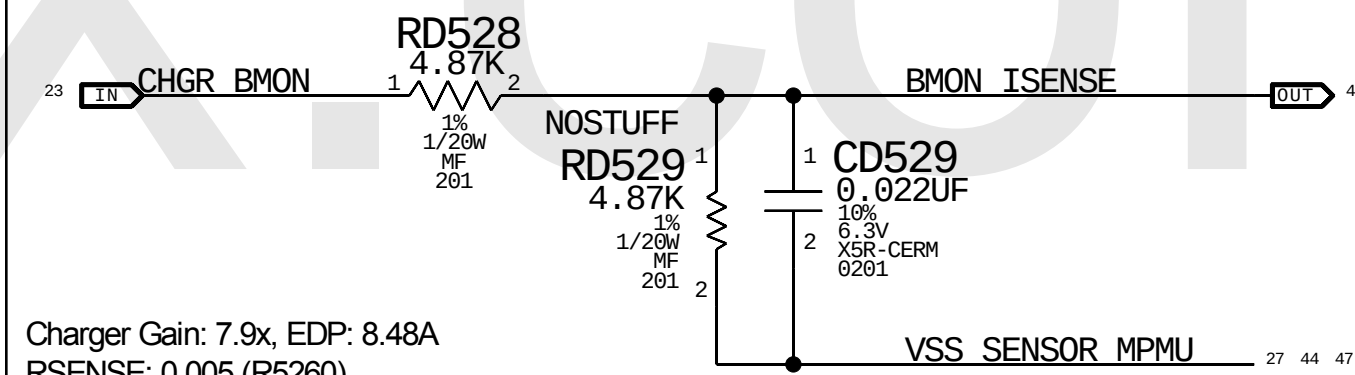
E DCIN Current Sensor (ID0R)

Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>



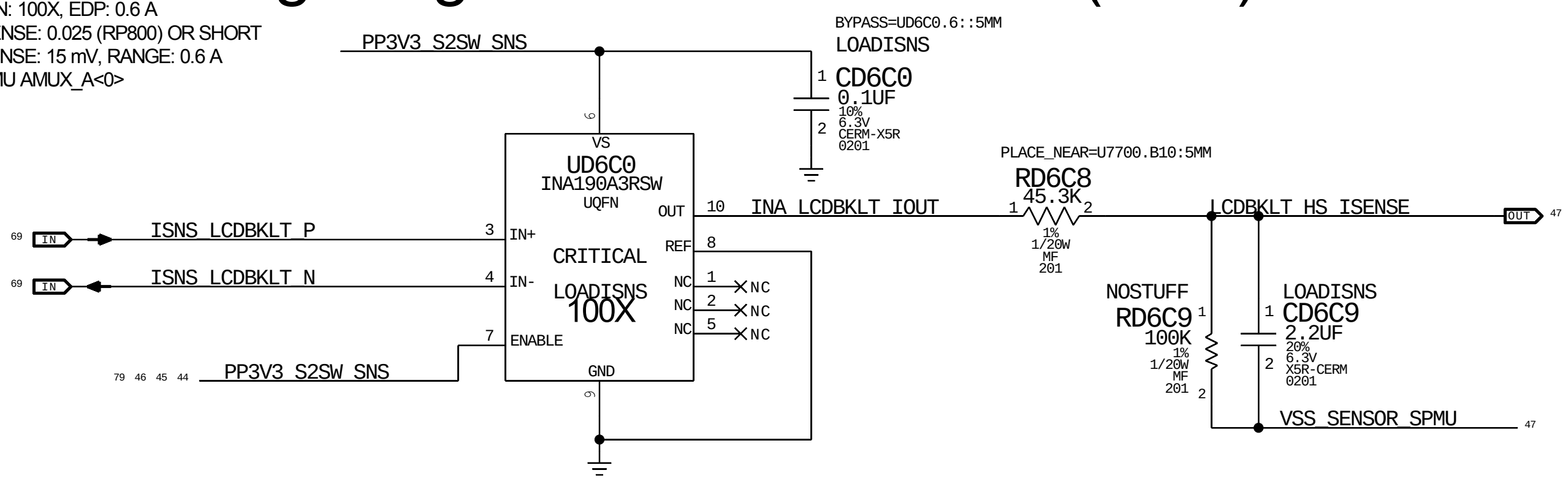
F BMON Current Sensor (IPBR)

Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>



A LCD Backlight High Side Current Sensor (IBLR)

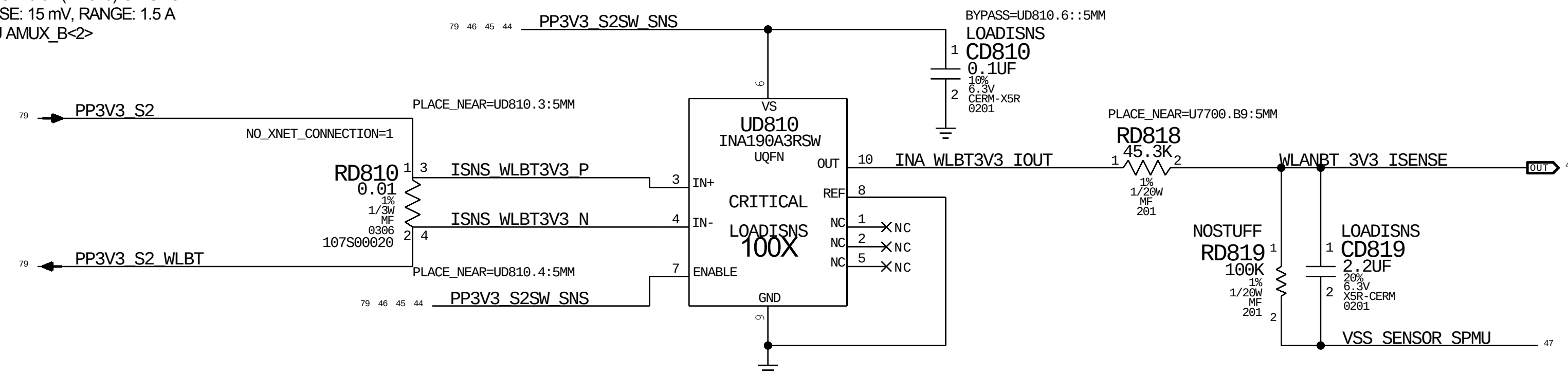
GAIN: 100X, EDP: 0.6 A
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 15 mV, RANGE: 0.6 A
SPMU AMUX_A<0>



Vinafix.com

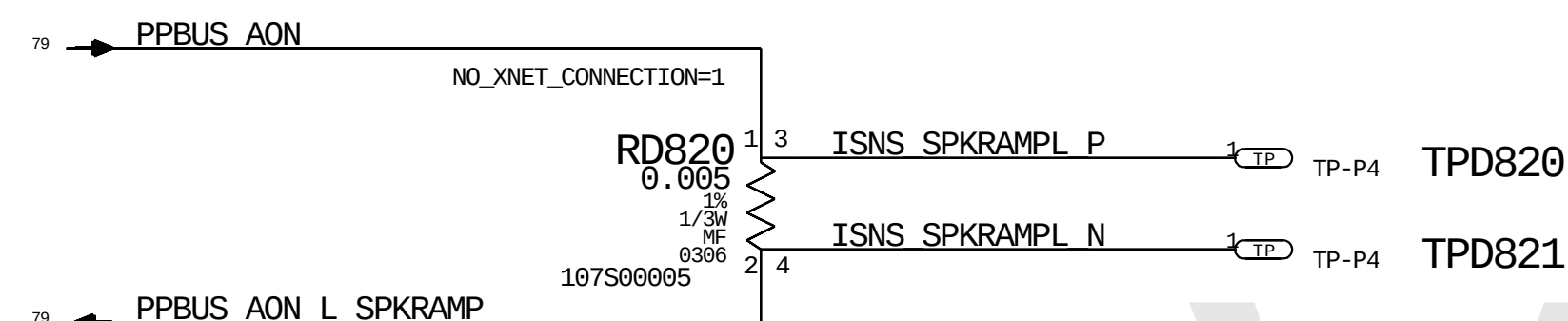
A WLAN BT 3V3 S2 Current Sensor (IW3C)

GAIN: 100X, EDP: 1.5 A
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 15 mV, RANGE: 1.5 A
SPMU AMUX_B<2>



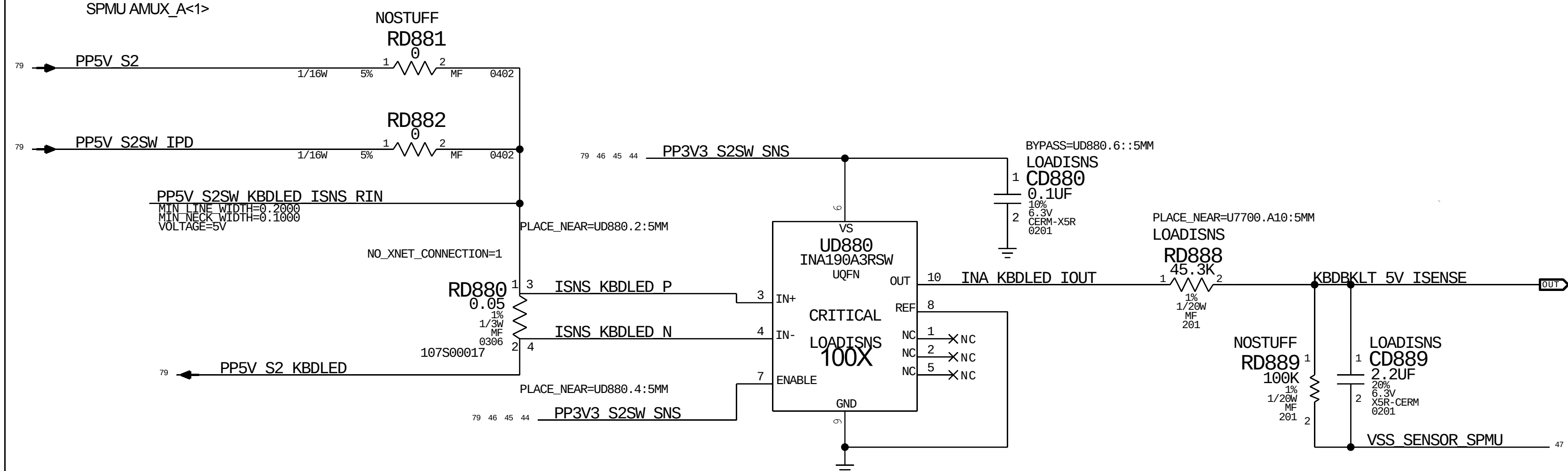
B Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



C Keyboard LED 5V Current Sensor (IKBC)

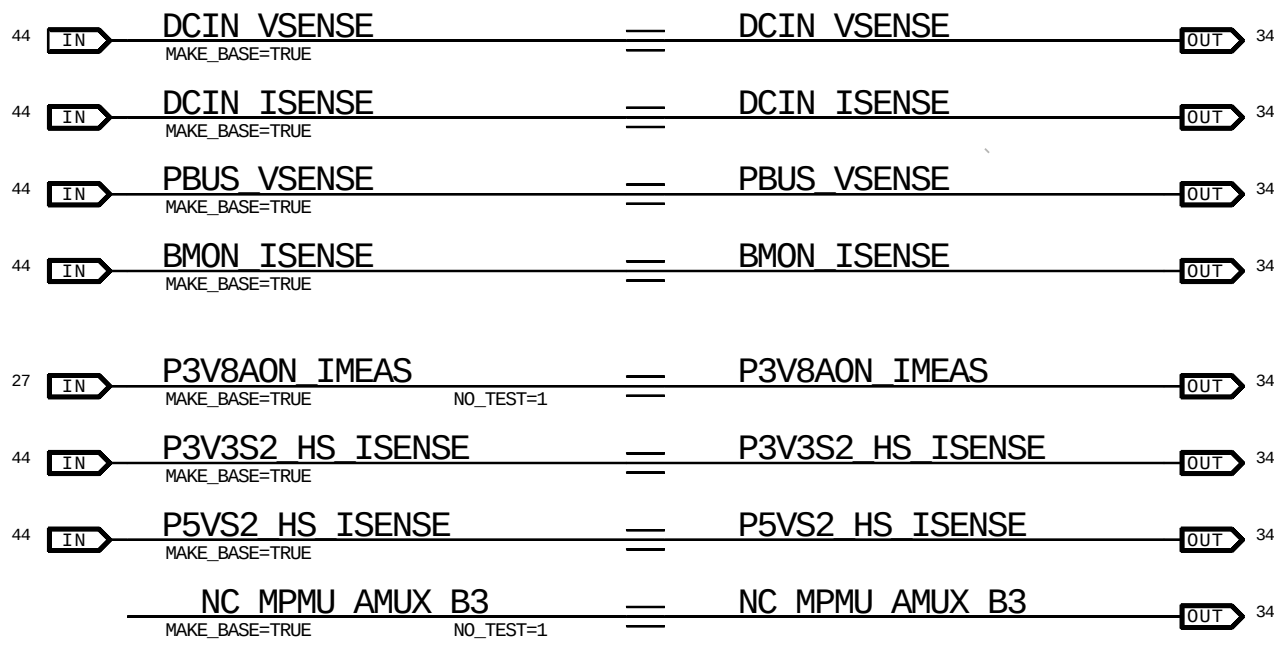
GAIN: 100X, EDP: 0.24 A
RSENSE: 0.05 (RD880) OR SHORT
VSENSE: 12 mV, RANGE: 0.33 A
SPMU AMUX_A<1>



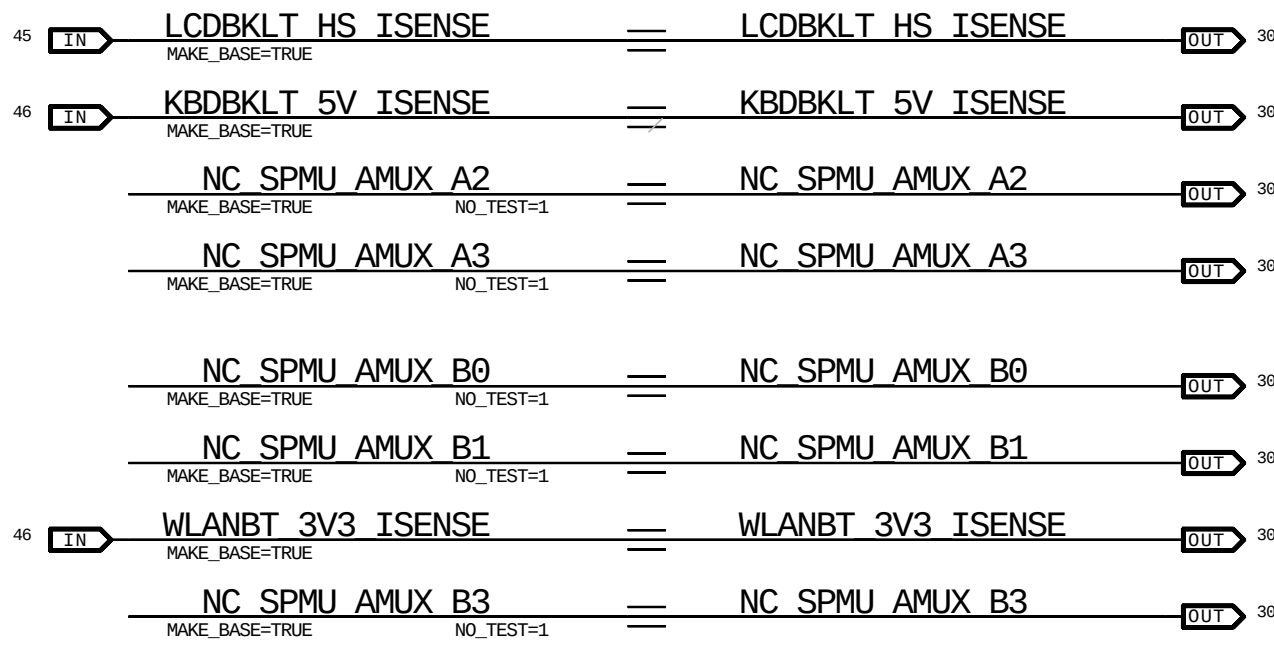
SENSORS: POWER LOW SIDE

A ADC Input Aliases

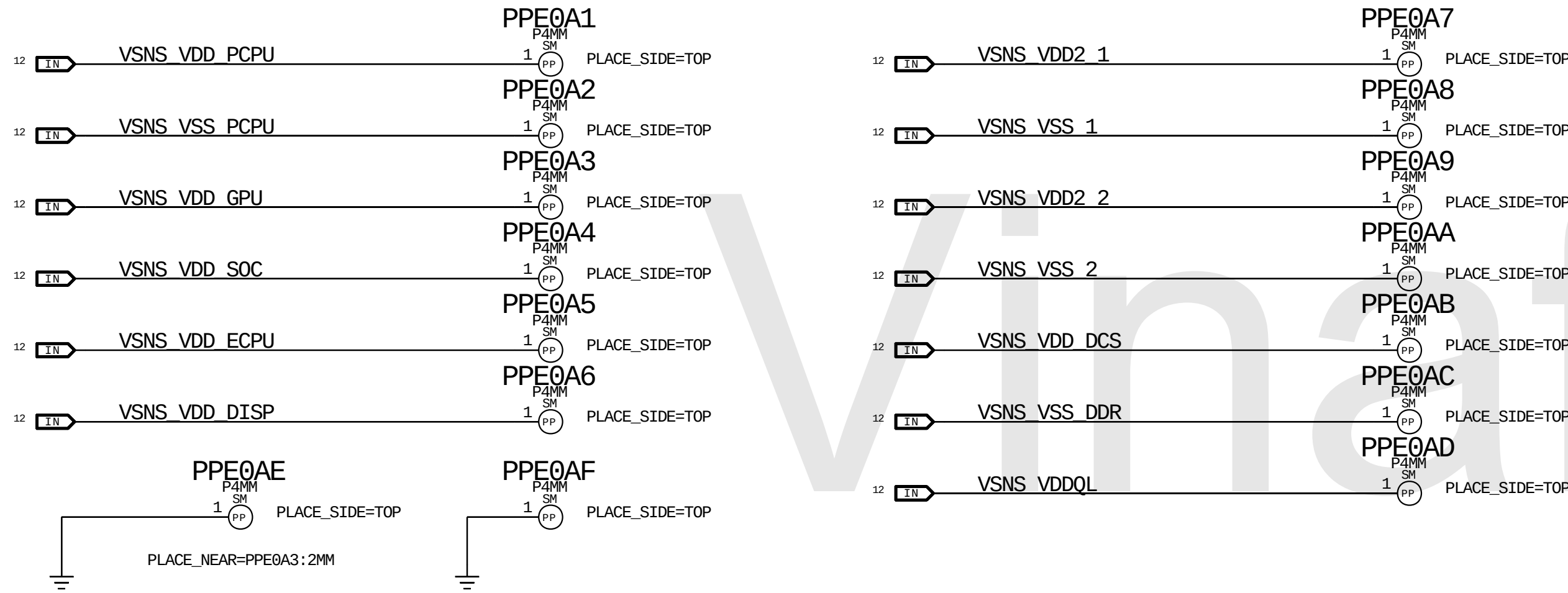
MASTER PMU AMUX ALIAS



SLAVE PMU AMUX ALIAS



B SOC Sense Lines

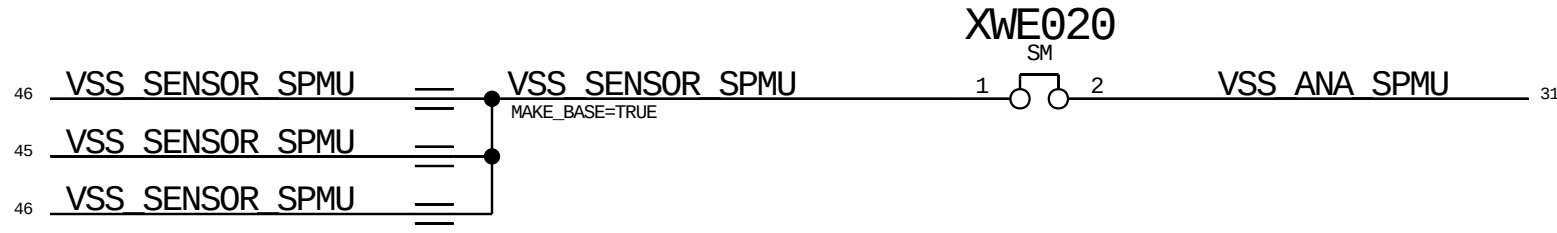


C I/V Sensor Ground Reference Aliases

Master PMU ADC Ground Alias

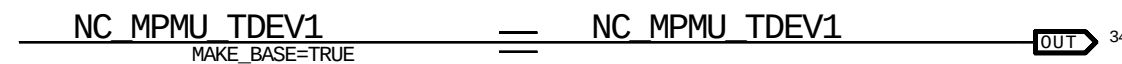


Slave PMU ADC Ground Alias



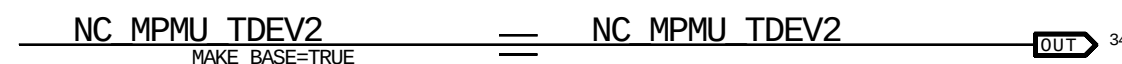
A Master PMU TDEV1 (Txxx)

Location: 3.8V AON VR



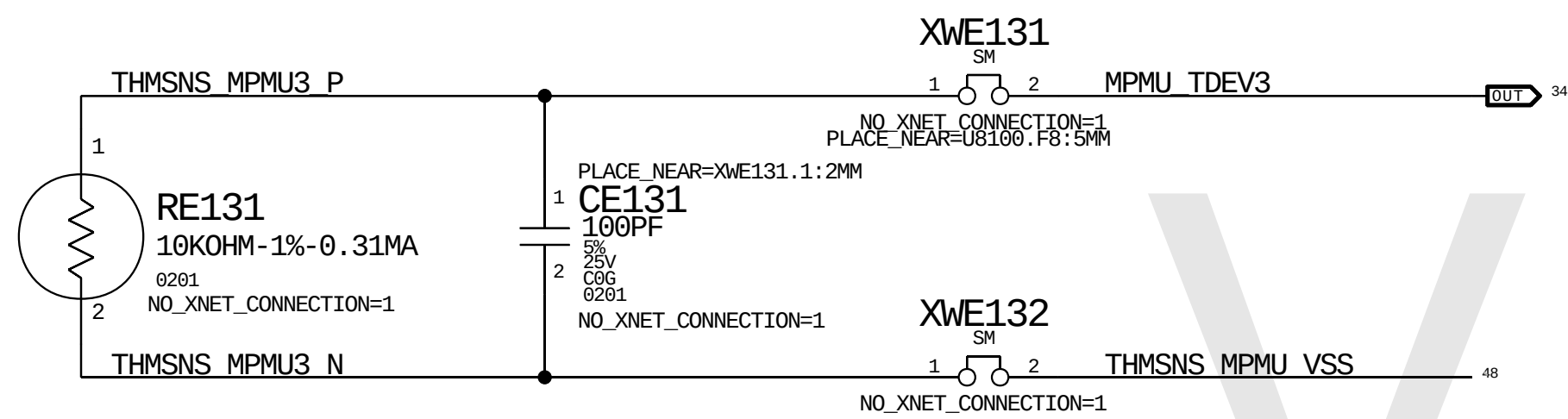
B Master PMU TDEV2 (Txxx)

Location: SoC back side ?



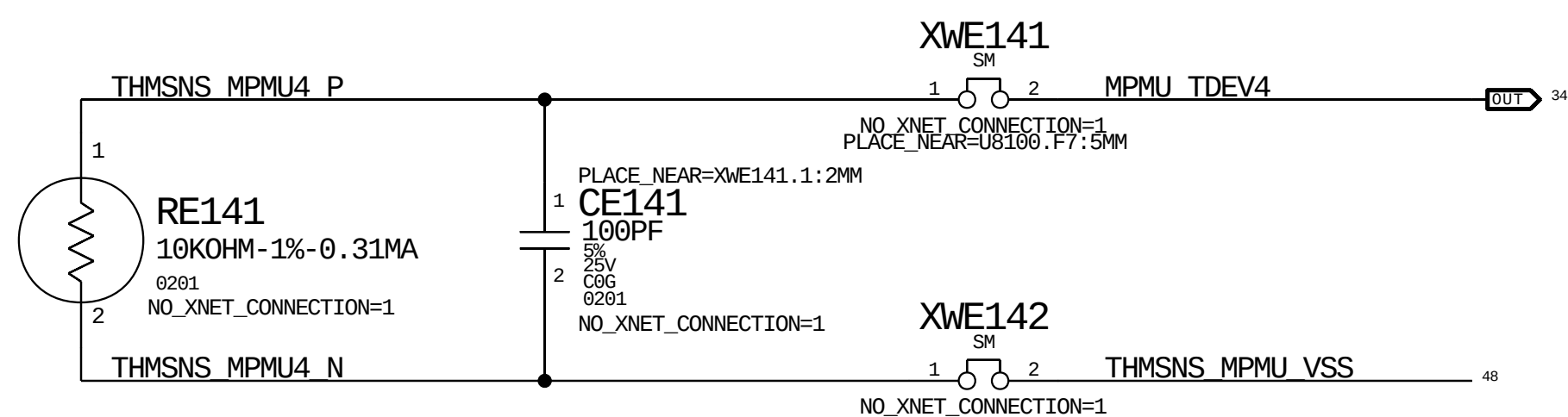
C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

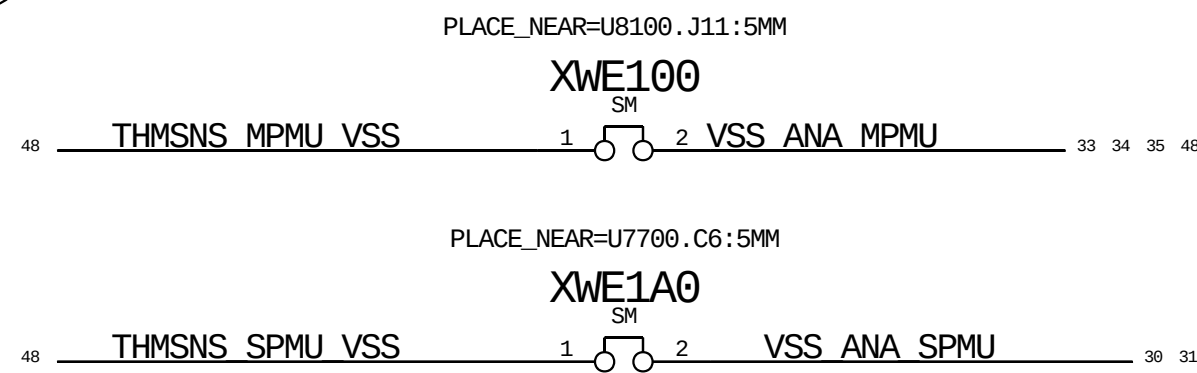


D Master PMU TDEV4 (TWOP)

Location: Wireless Proximity

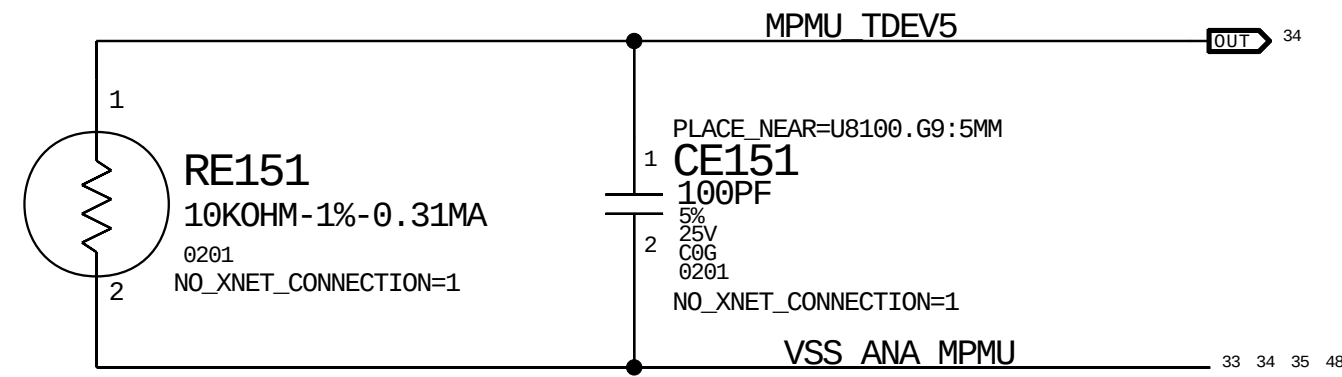


E Master/Slave PMU VSS Connection



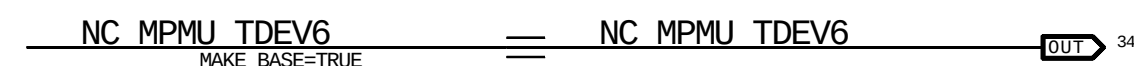
F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity



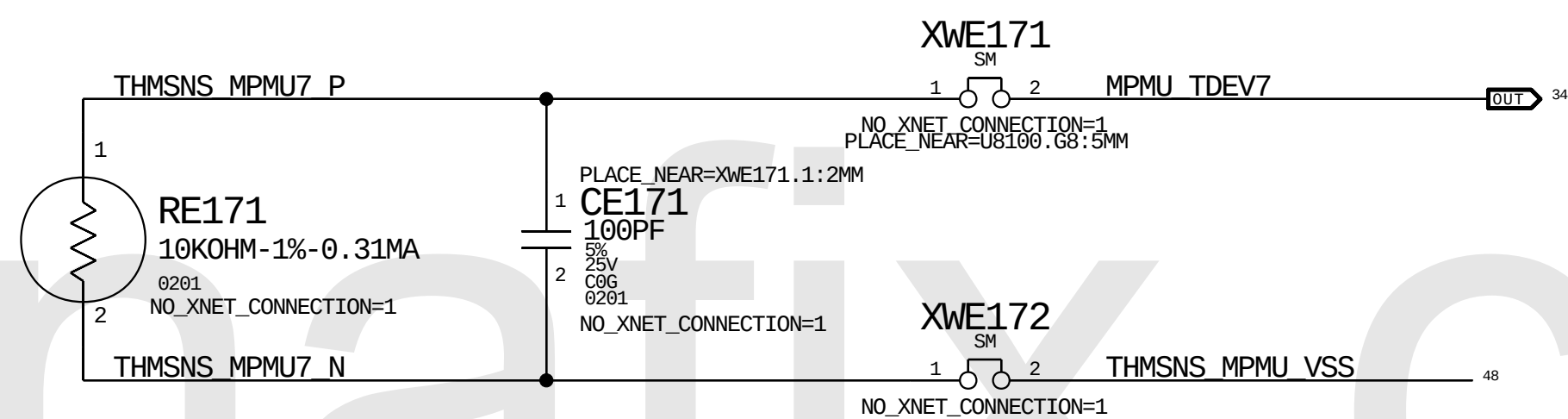
G Master PMU TDEV6 (Txxx)

Location: NAND, TBD



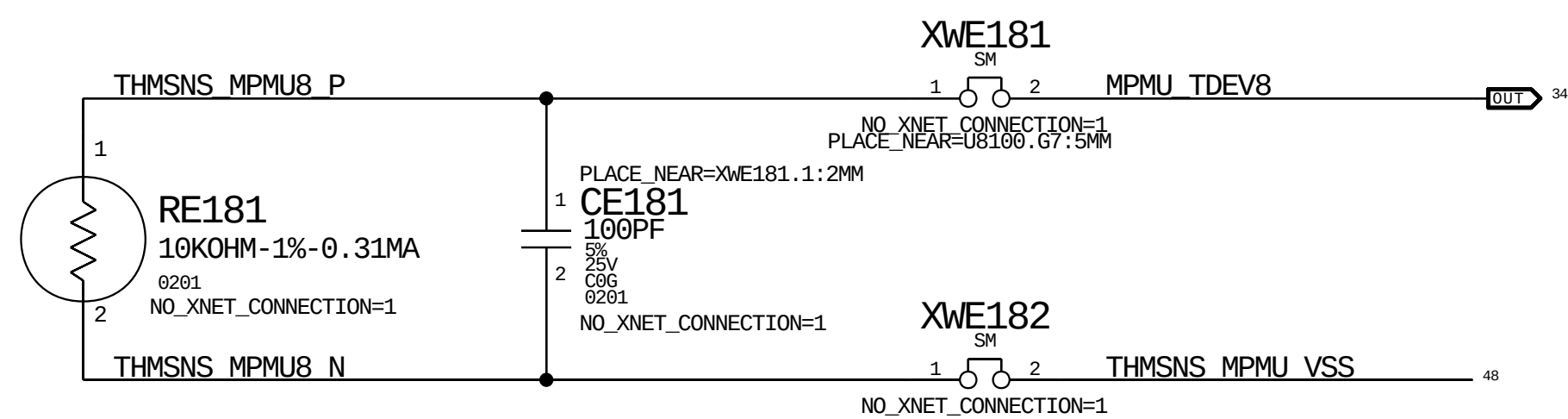
H Master PMU TDEV7 (TCHP)

Location: Charger Proximity



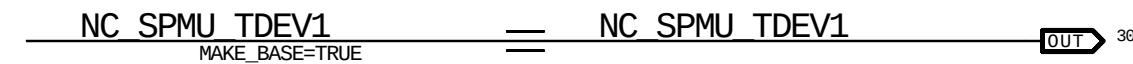
I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)



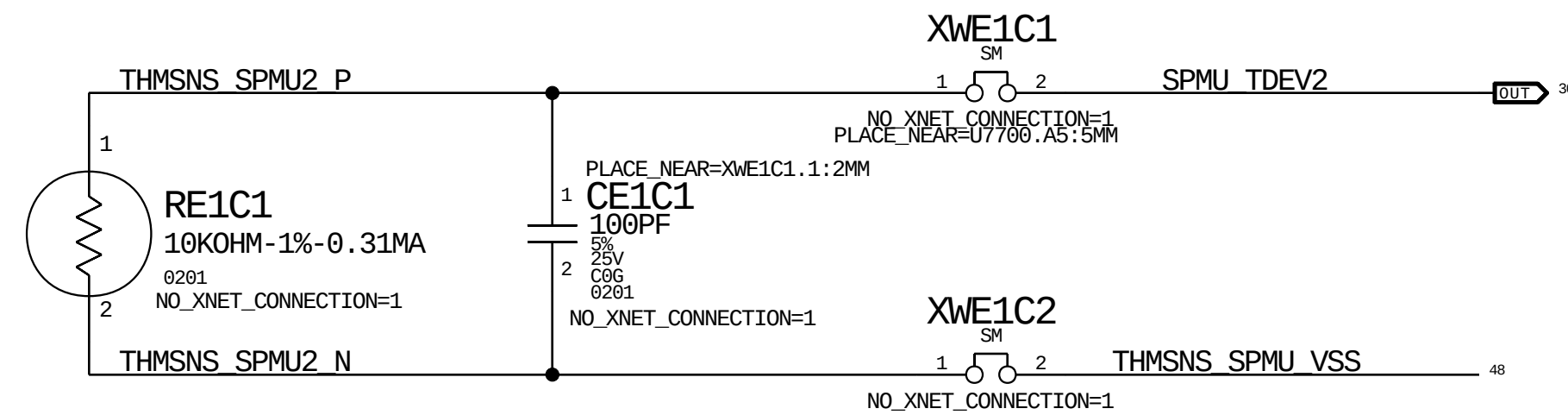
J Slave PMU TDEV1 (Txxx)

Location: TBD



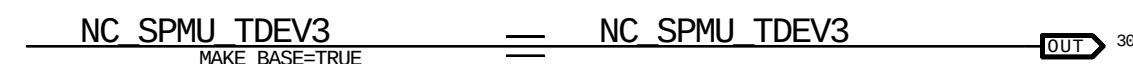
K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity



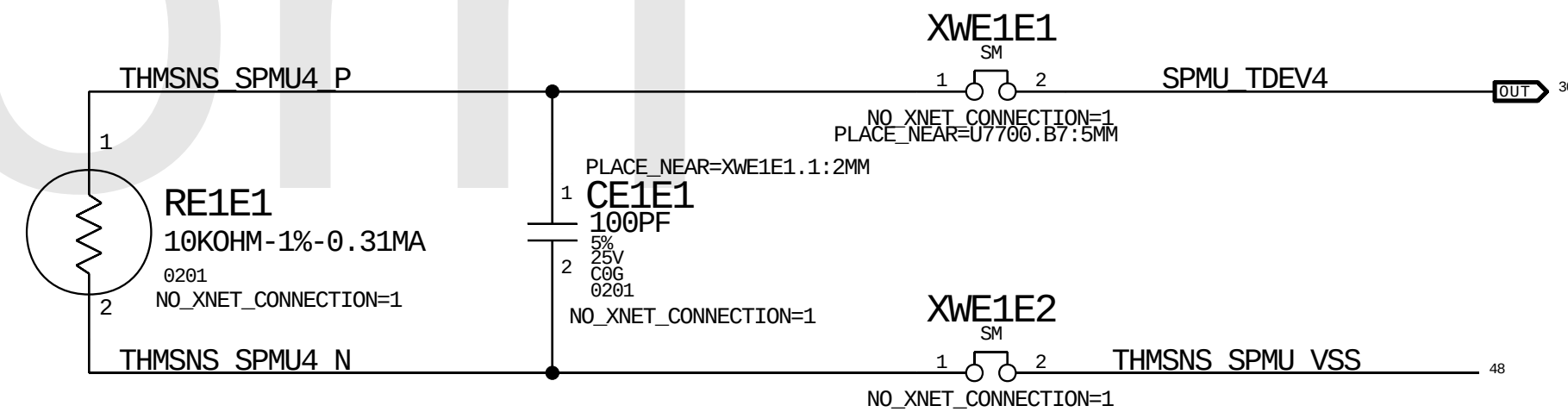
L Slave PMU TDEV3 (Txxx)

Location: TBD



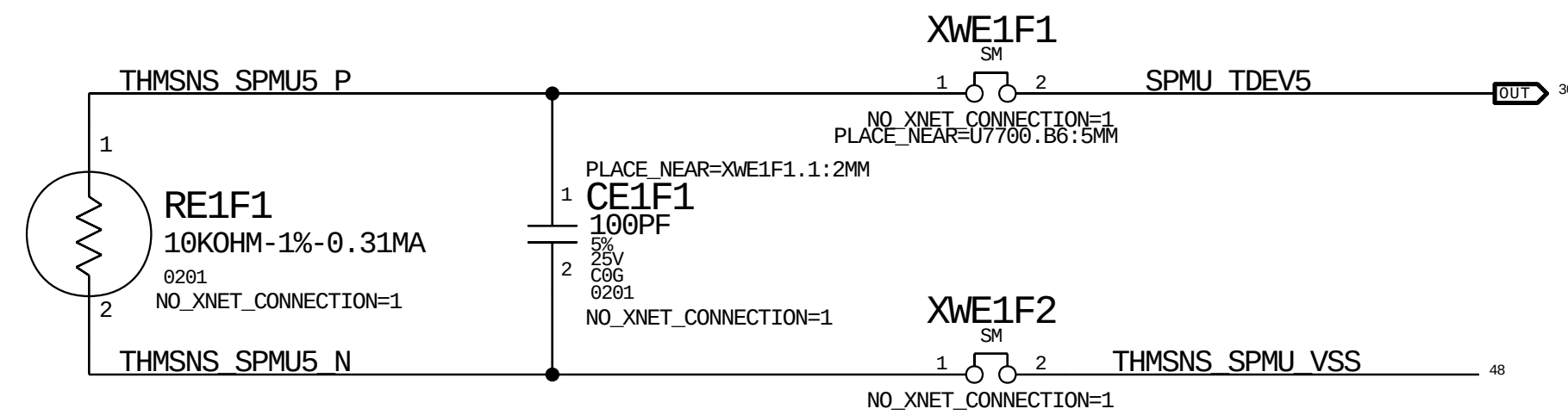
M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity



N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity

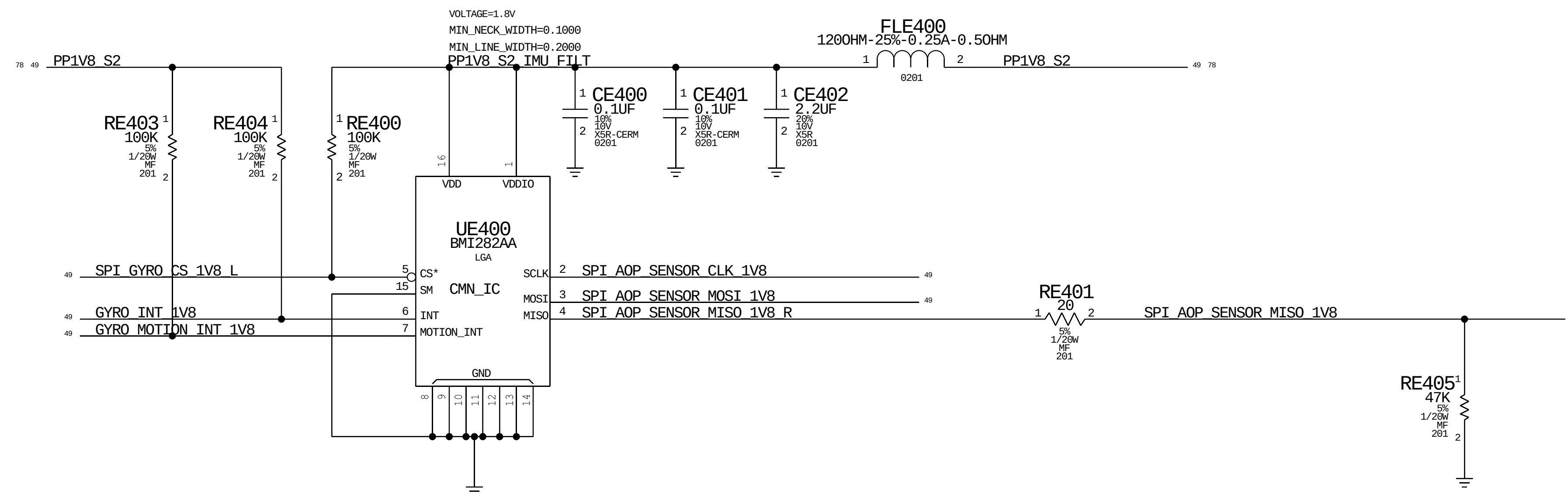


Sensors: Thermal

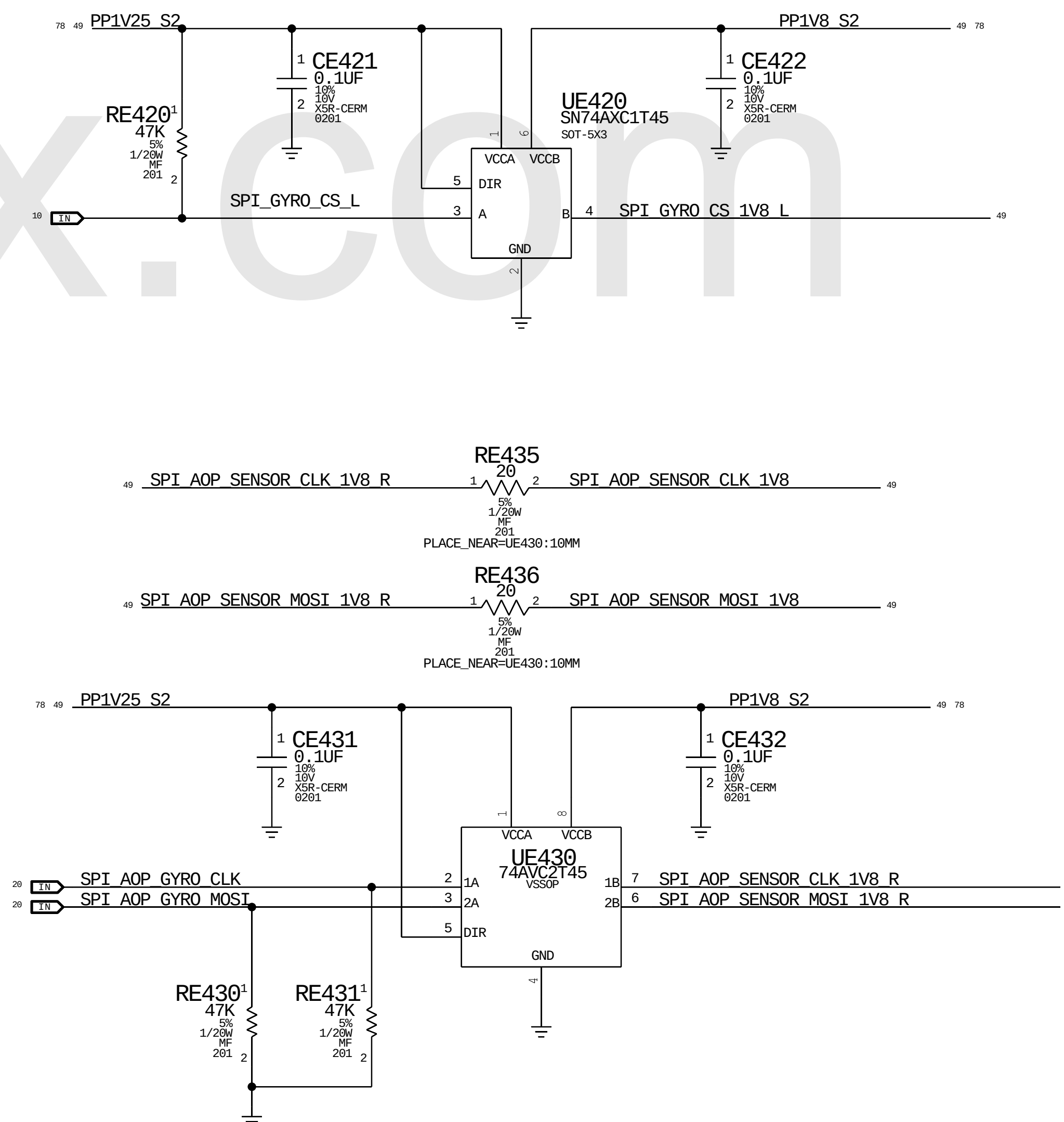
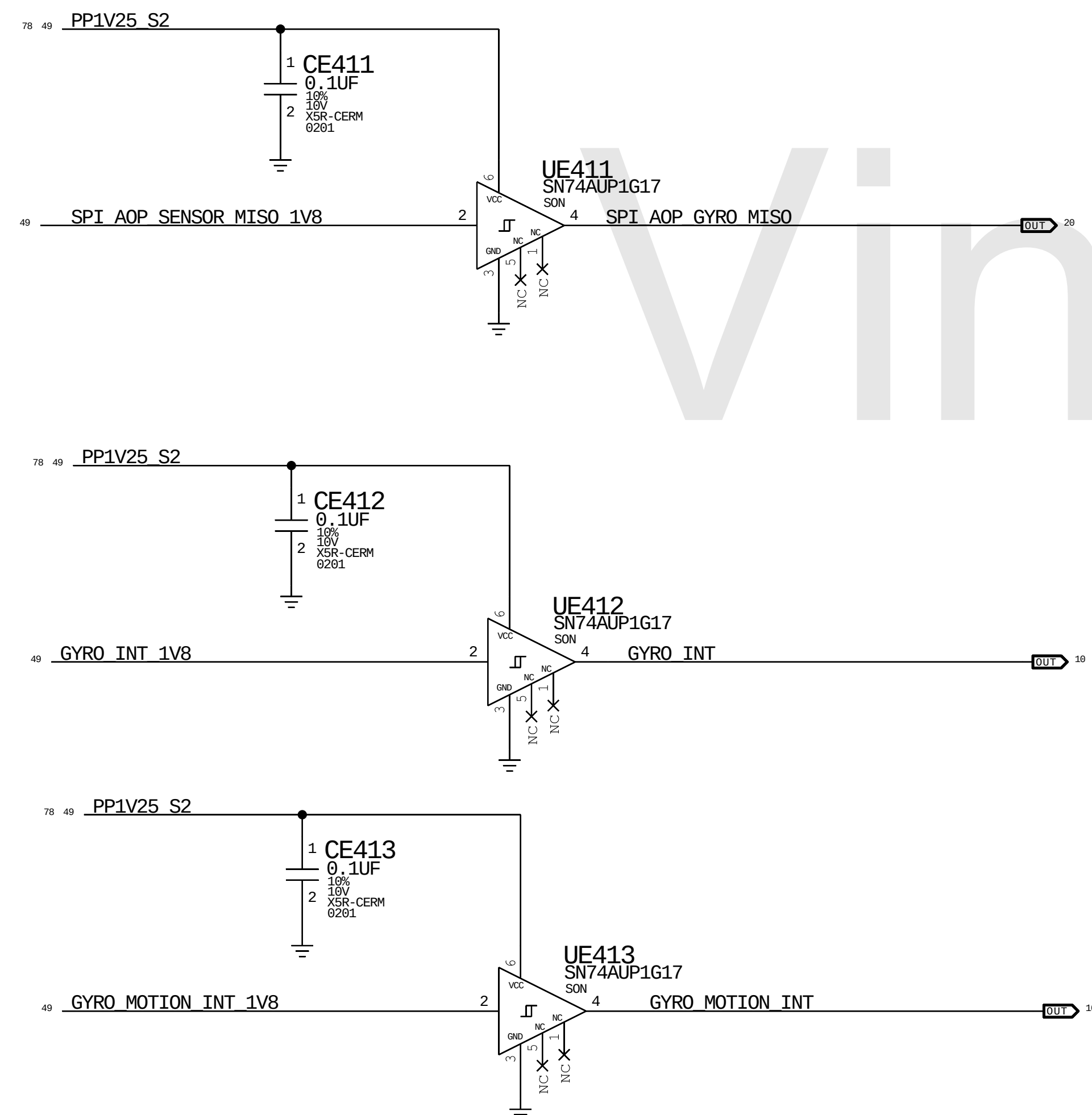
OPEN ITEMS:

FERRITE IS PLACEHOLDER ONLY
J417 USES 1555S0686 (01005)
MUST FIND PROPER PART, IF ONE IS NEEDED AT ALL
WHAT DOES SM SCAN MODE PIN DO AND WHY IS IT GROUNDED ON J417?

KOBOL: ACCEL & GYRO

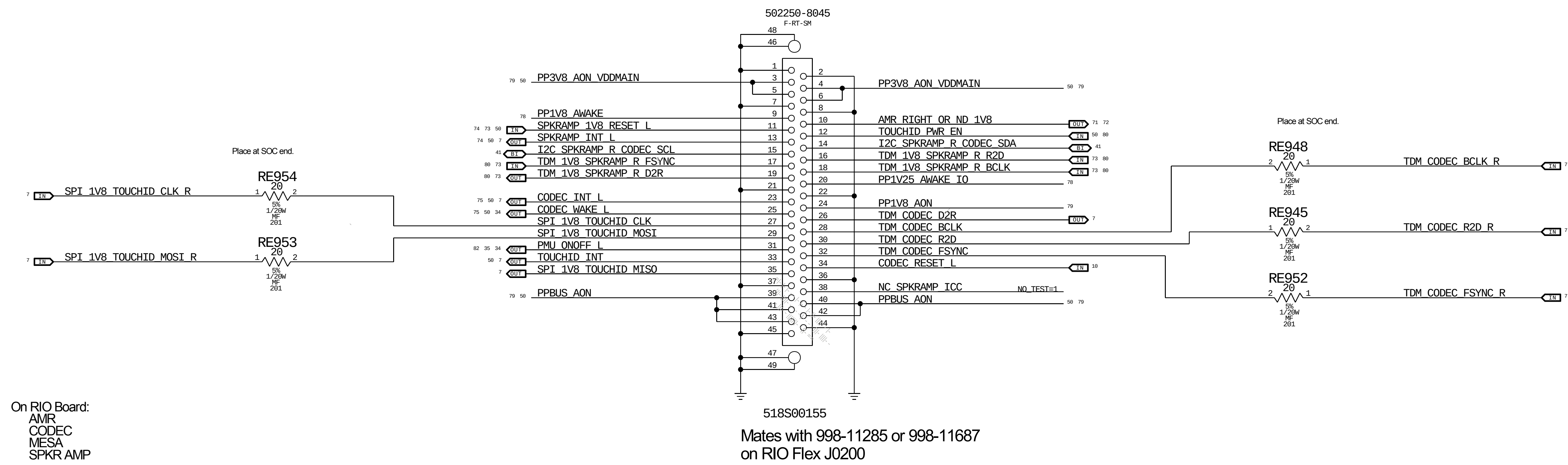


SPI LEVEL TRANSLATION

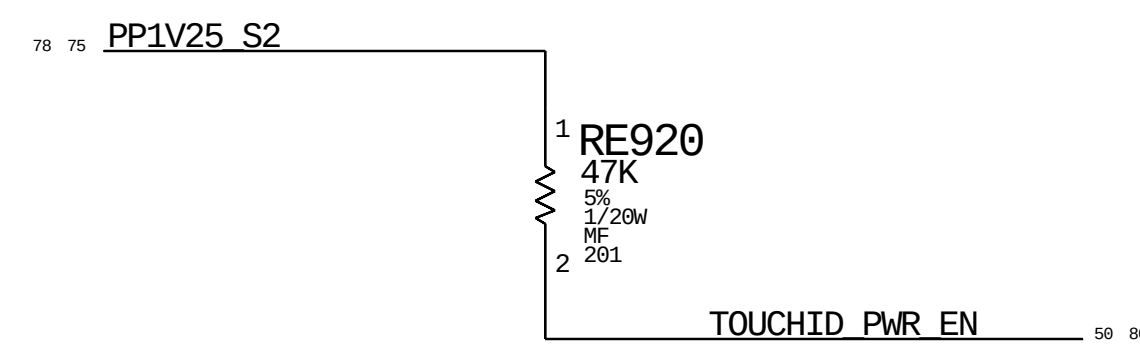


SENSORS: MOTION

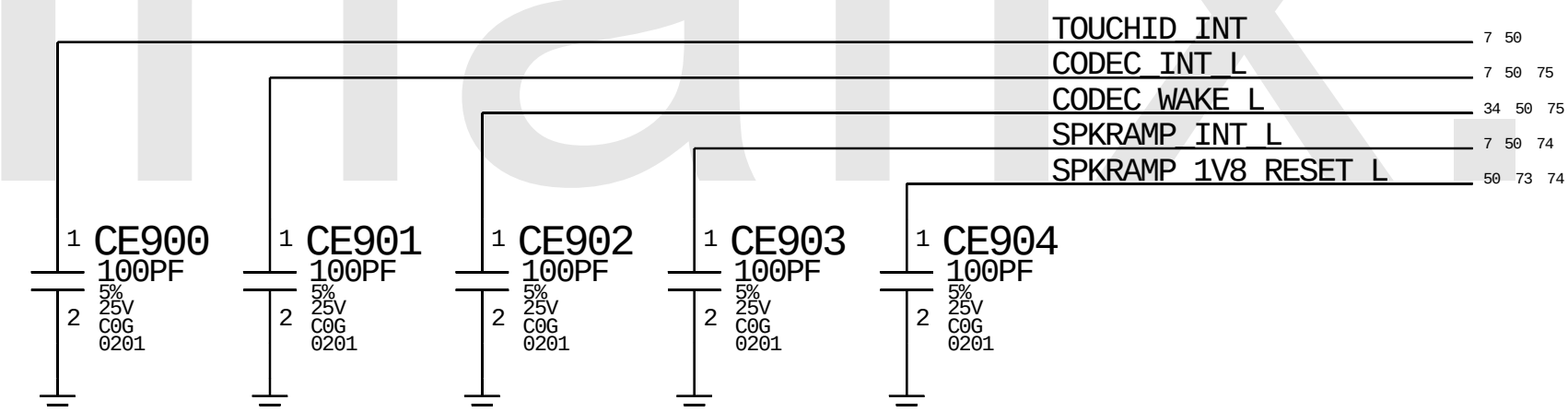
RIO Board Connector



B TOUCHID Power Enable Pull-Up

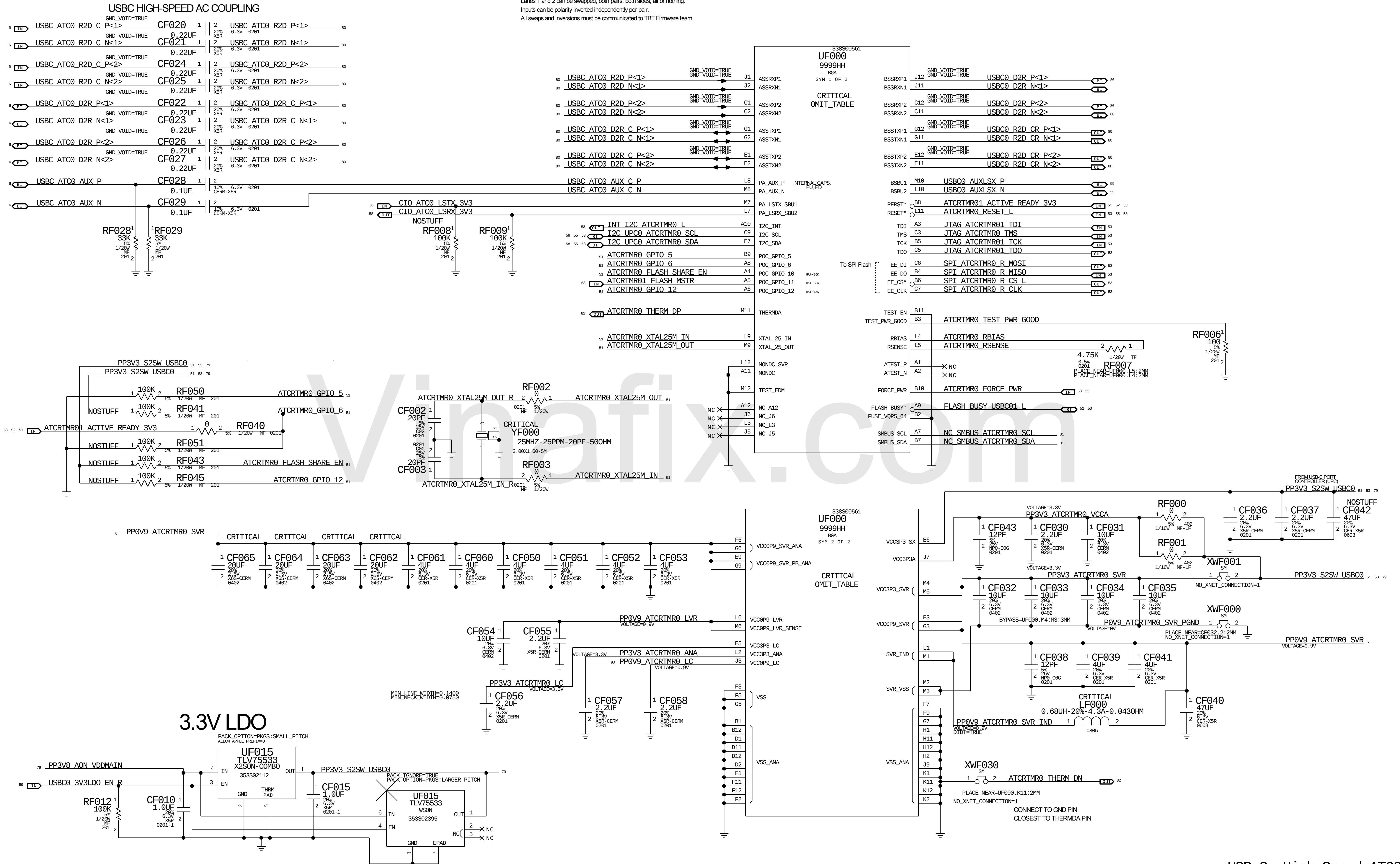


C RIO Control Capacitors



```
** OK2INTEGRATE **
```

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

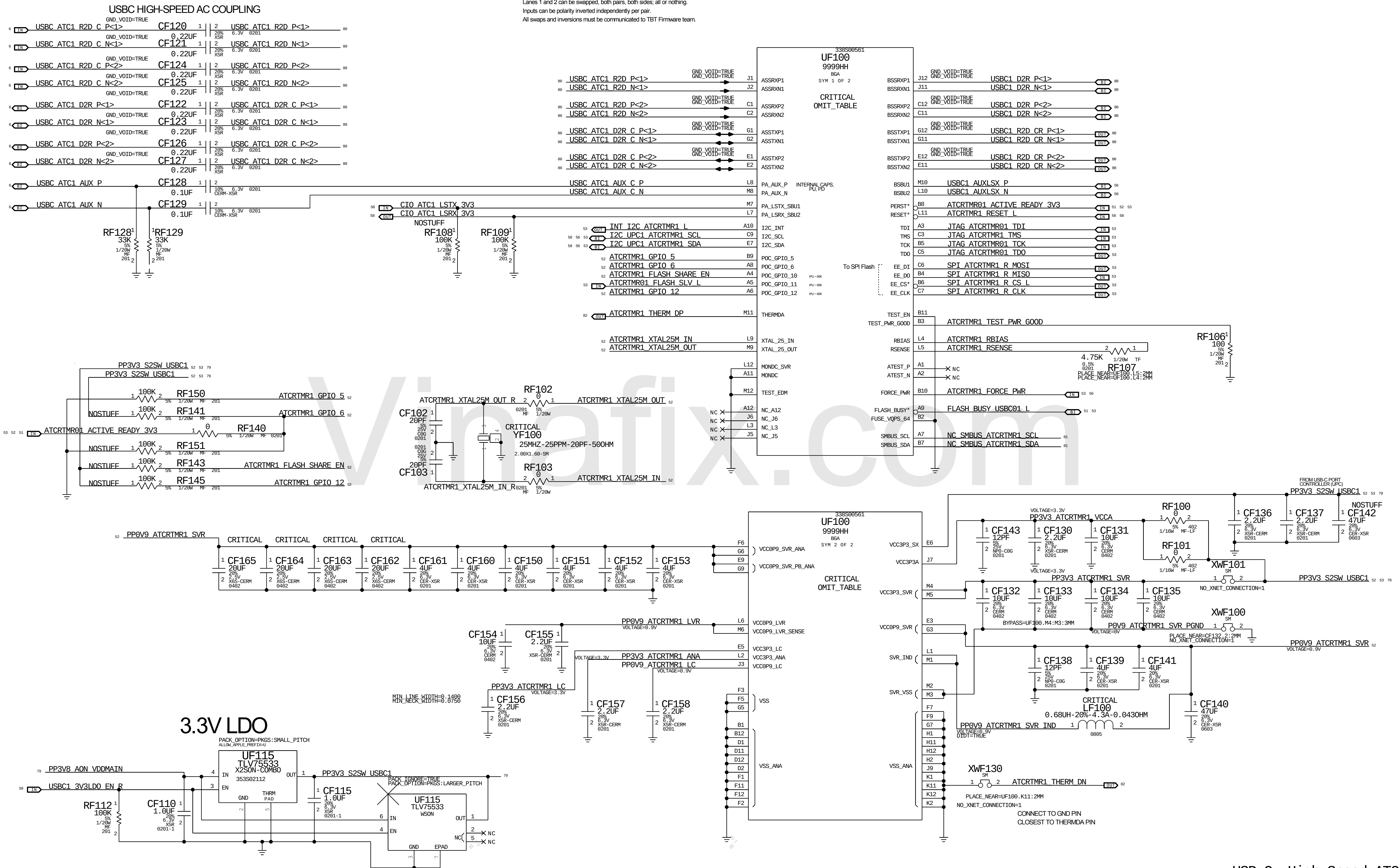


USB-C: High Speed ATC0

BOM_COST_GROUP=TBT

** OK2INTEGRATE **

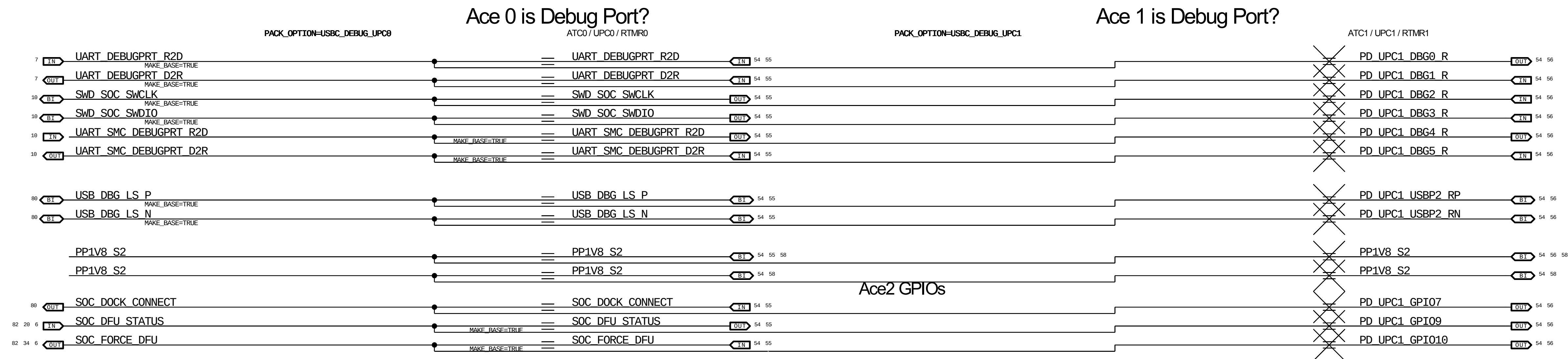
Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.



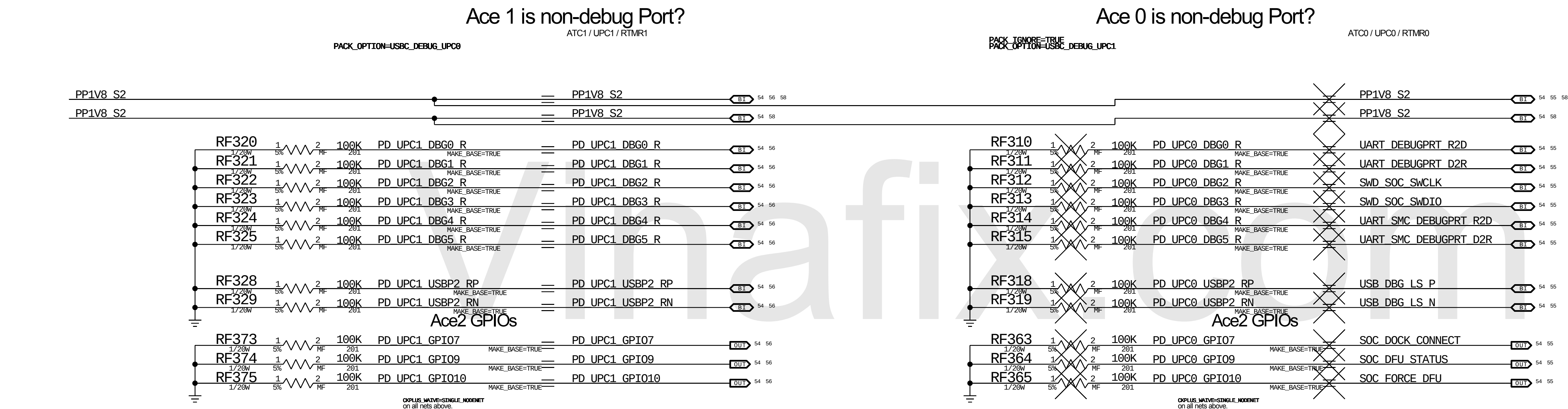
USB-C: High Speed ATC1

BOM_COST_GROUP=TBT

** OK2INTEGRATE **

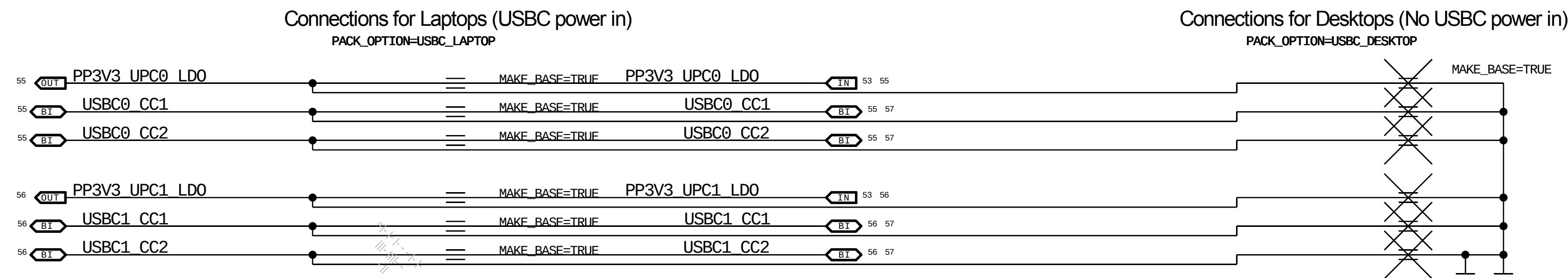
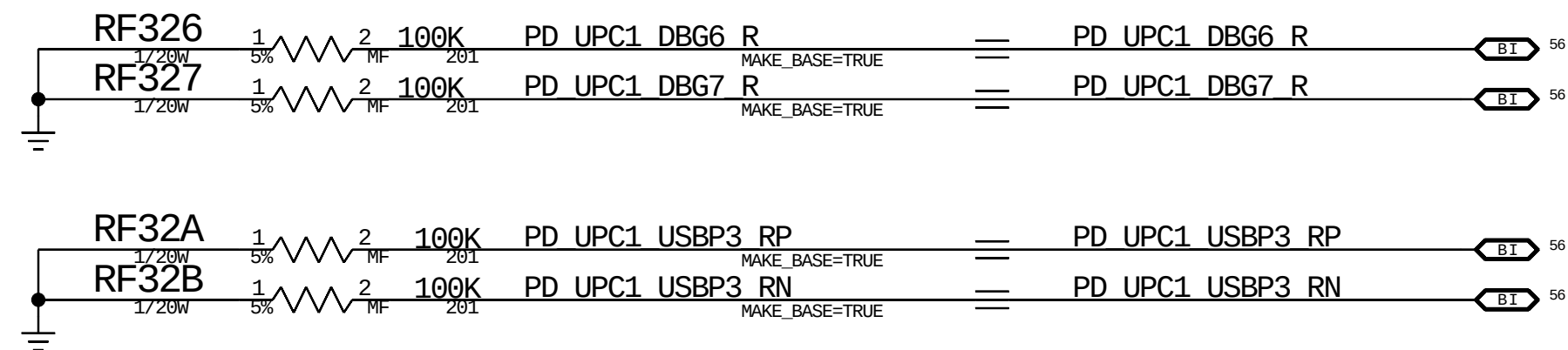
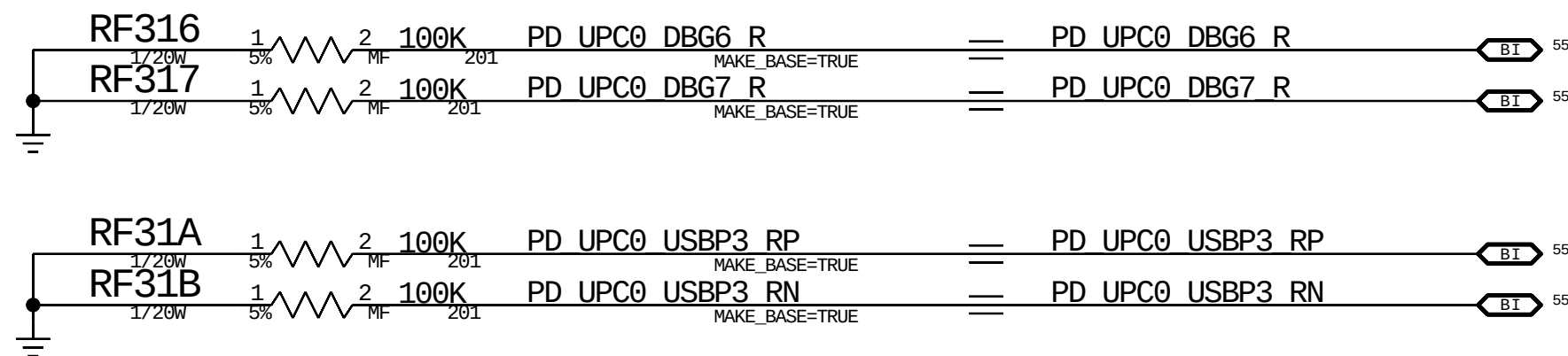


Main Debug Port



Non-debug Port

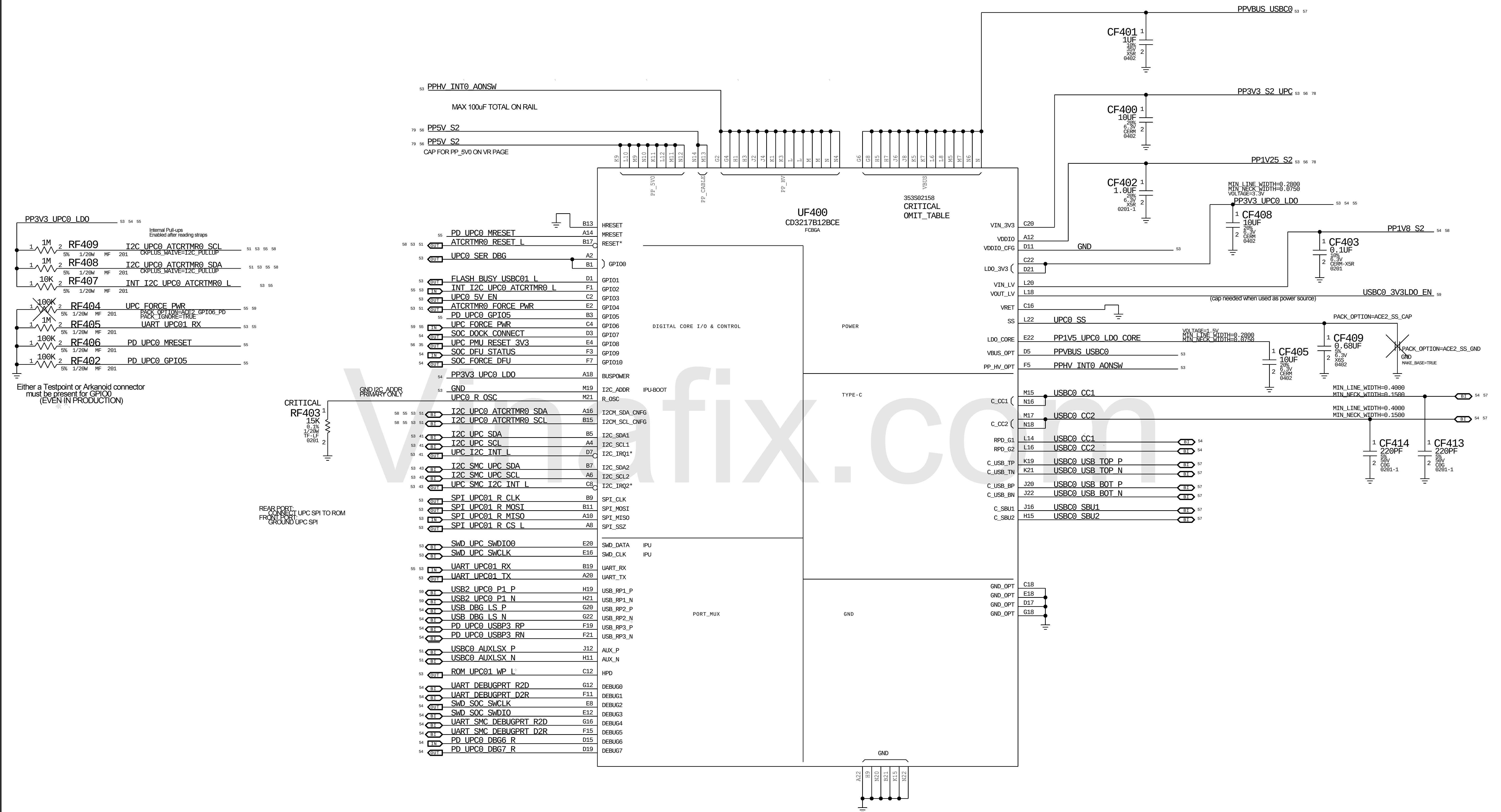
Unused ports



BOM_COST_GROUP=USB-C

USB-C: Support 2 ATC01

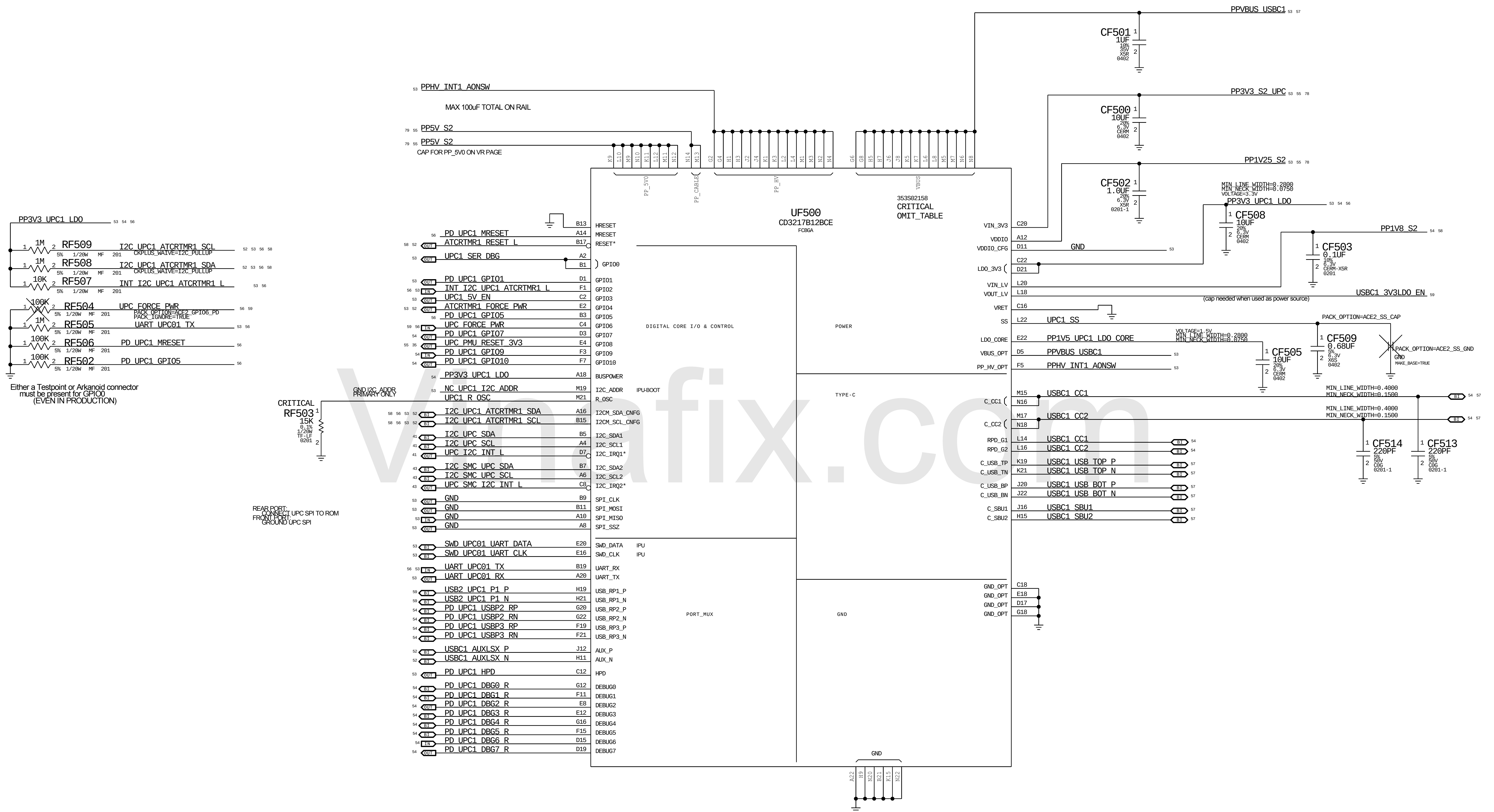
** OK2INTEGRATE **



BOM_COST_GROUP=USB-C

USB-C: Port Controller ATC0

** OK2INTEGRATE **



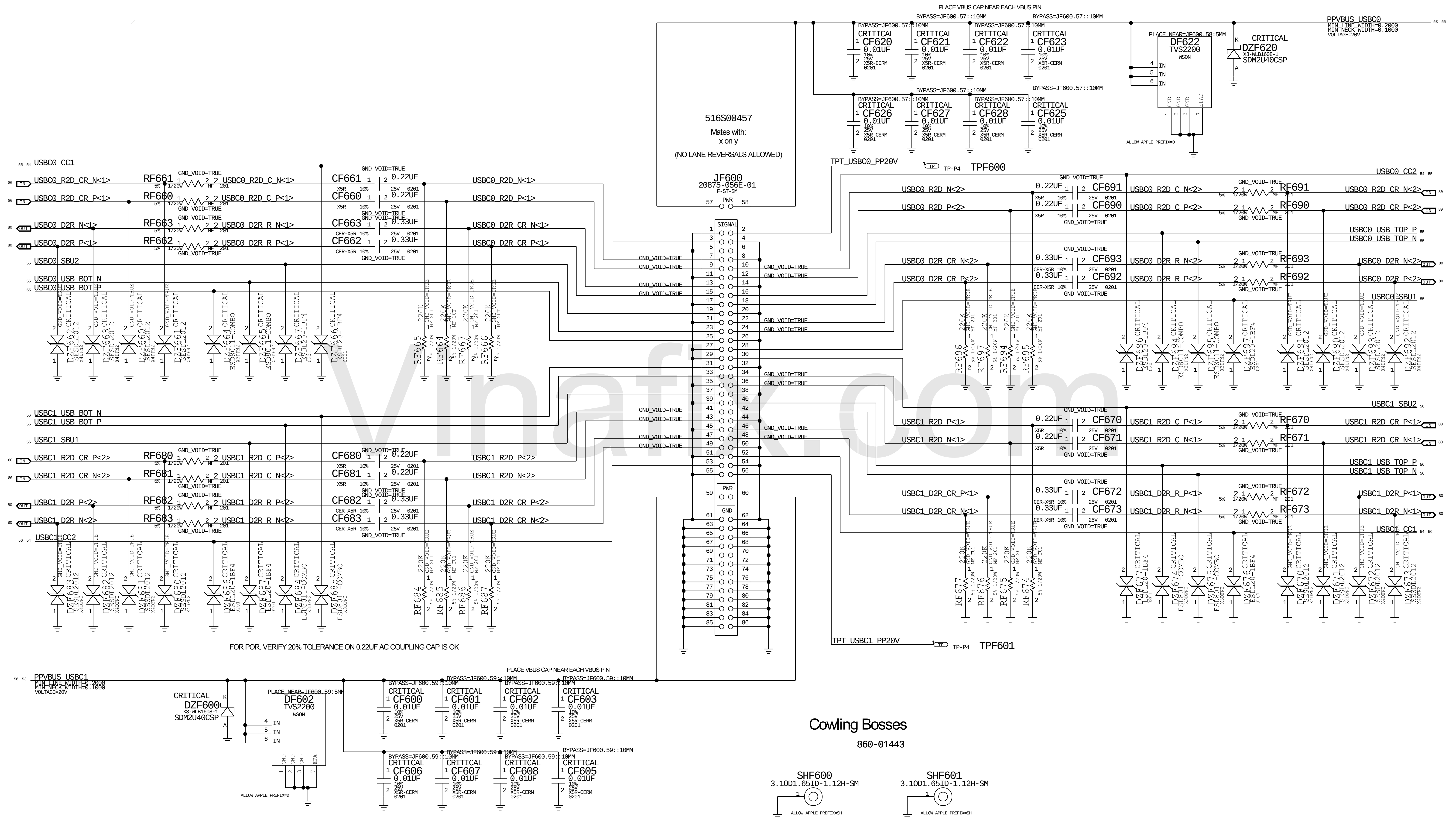
BOM_COST_GROUP=USB-C

USB-C: Port Controller ATC1

----- Reference only -----

Left Rear Port

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

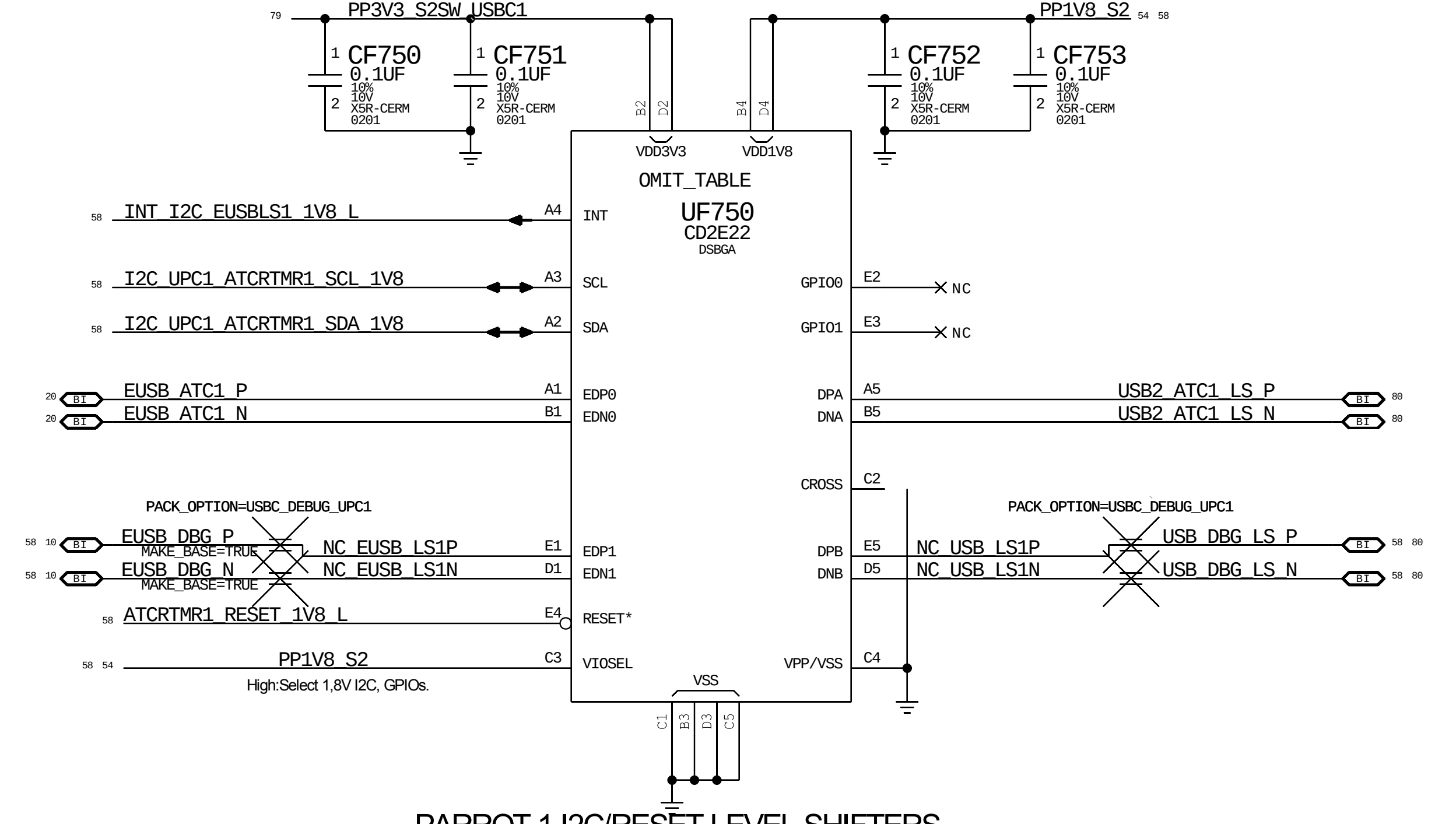
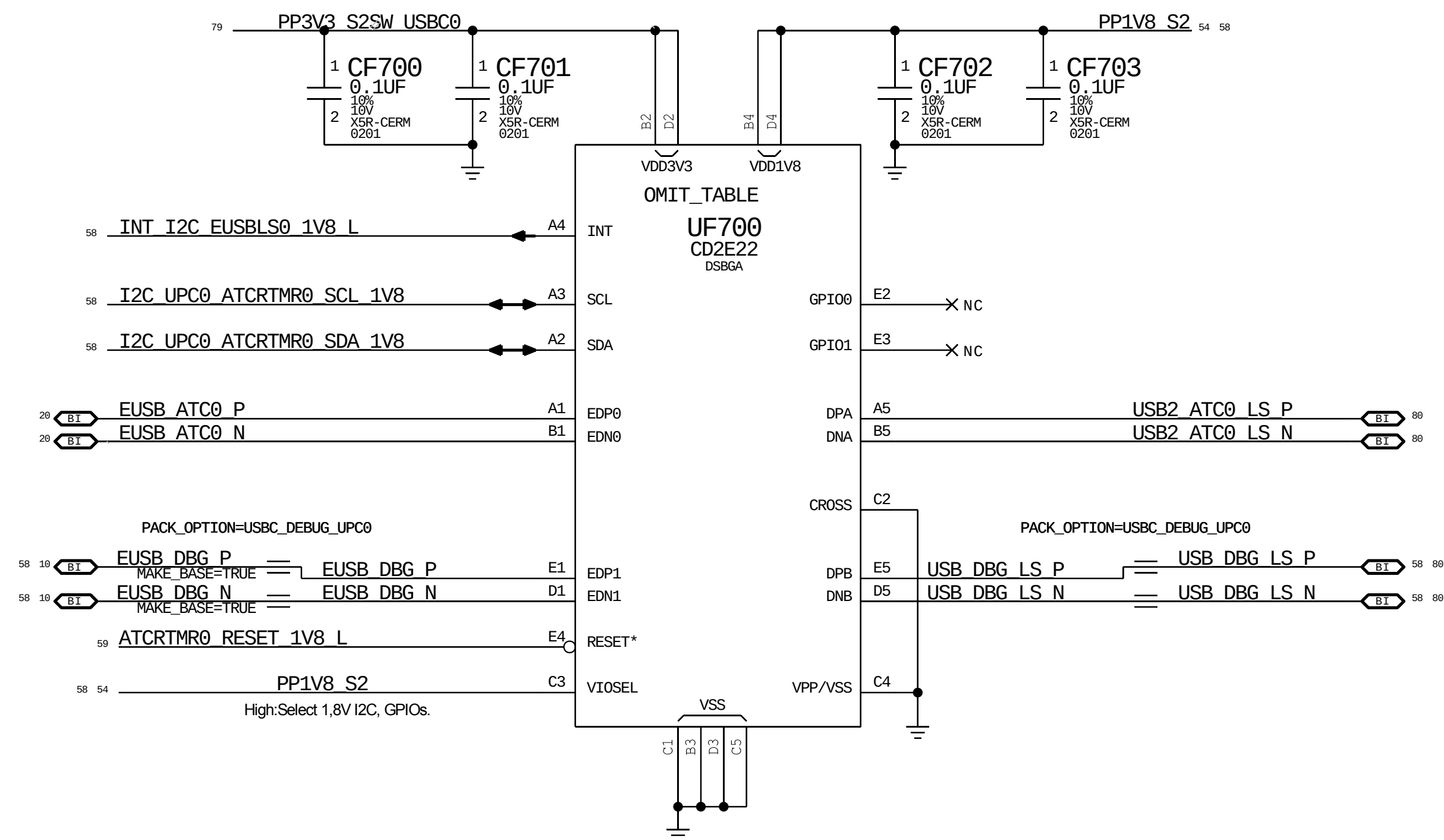


Left Front Port

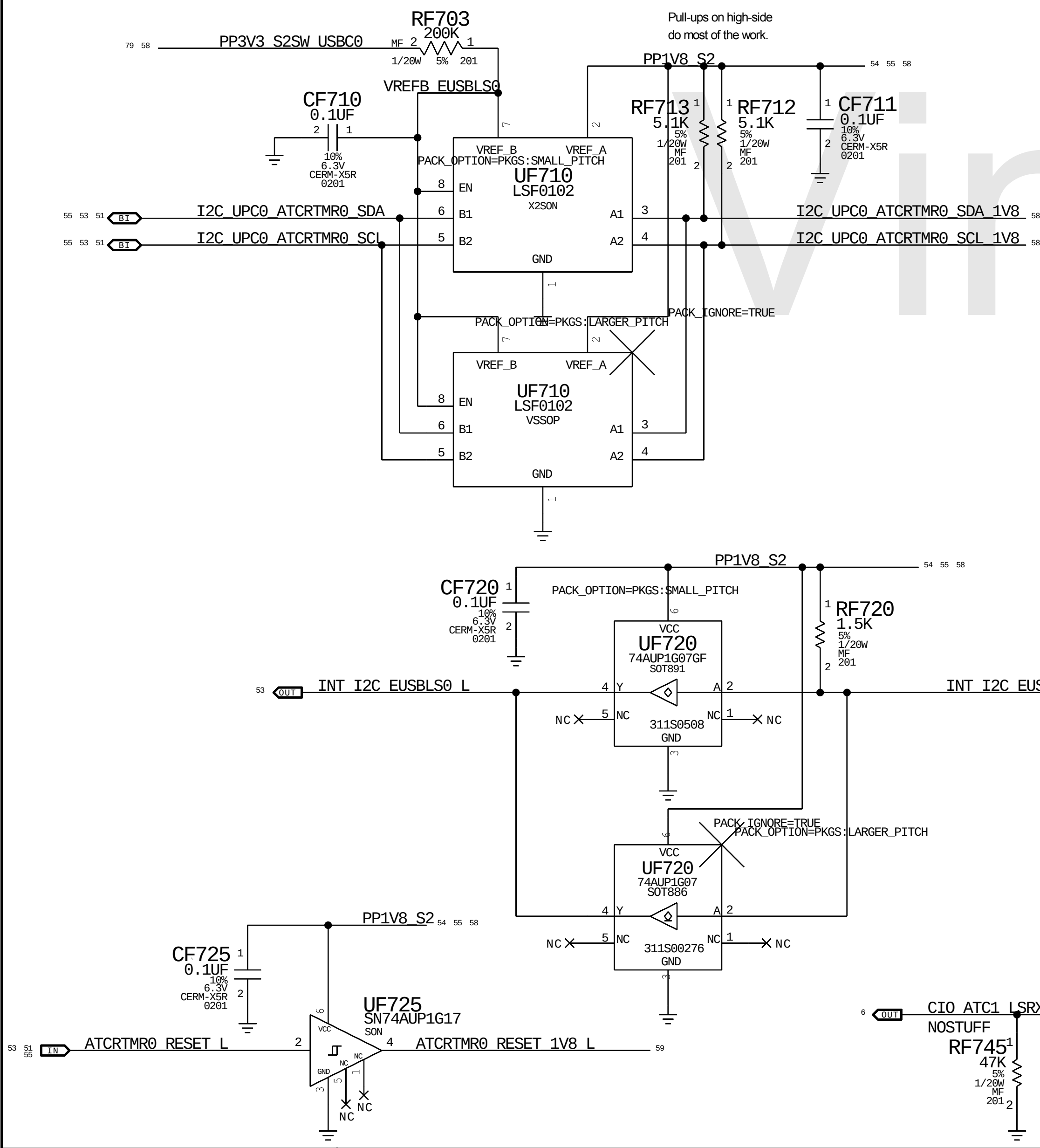
USB-C: Connector(s)

BOM_COST_GROUP=USB-C

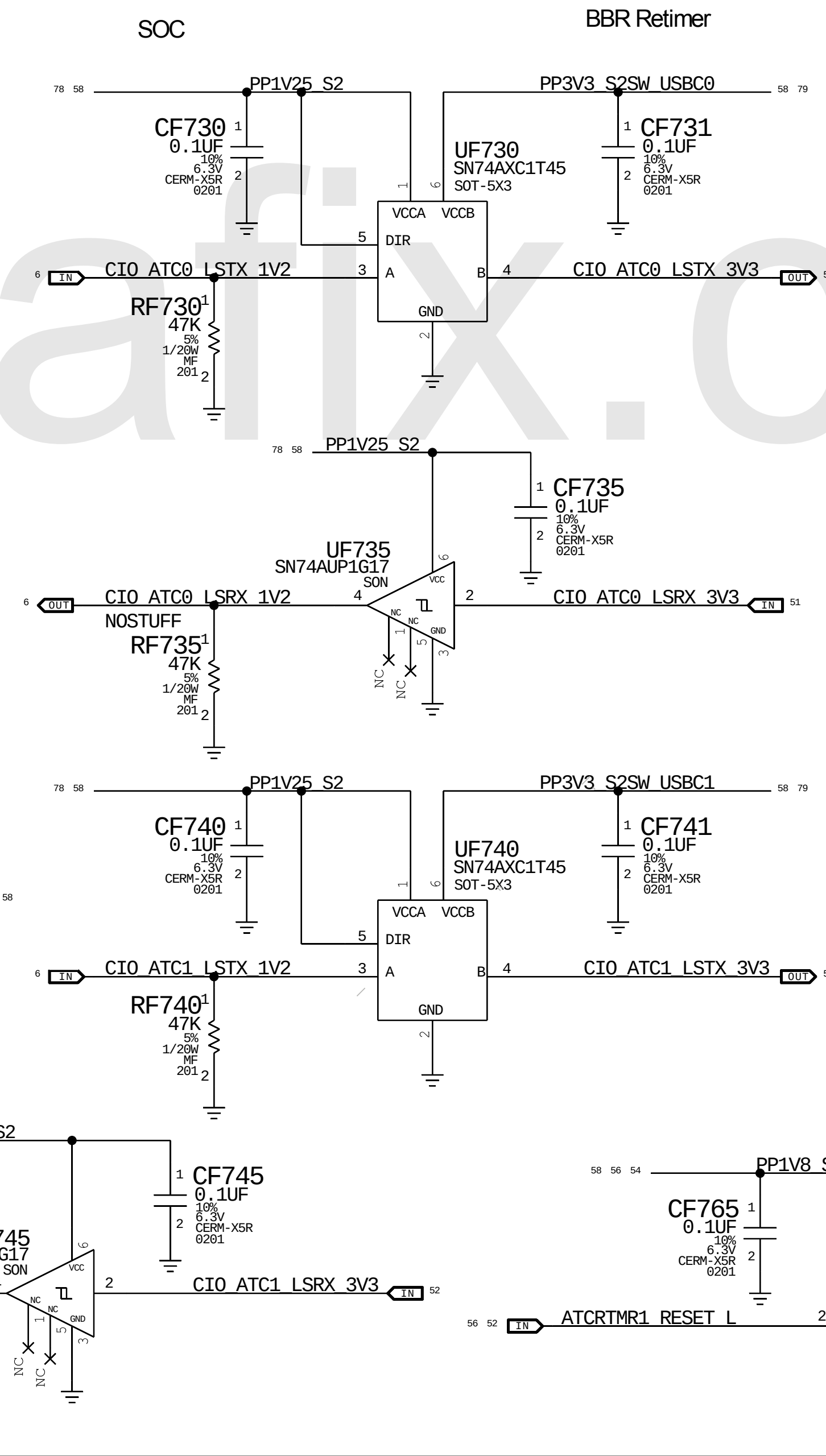
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** OK2INTEGRATE **
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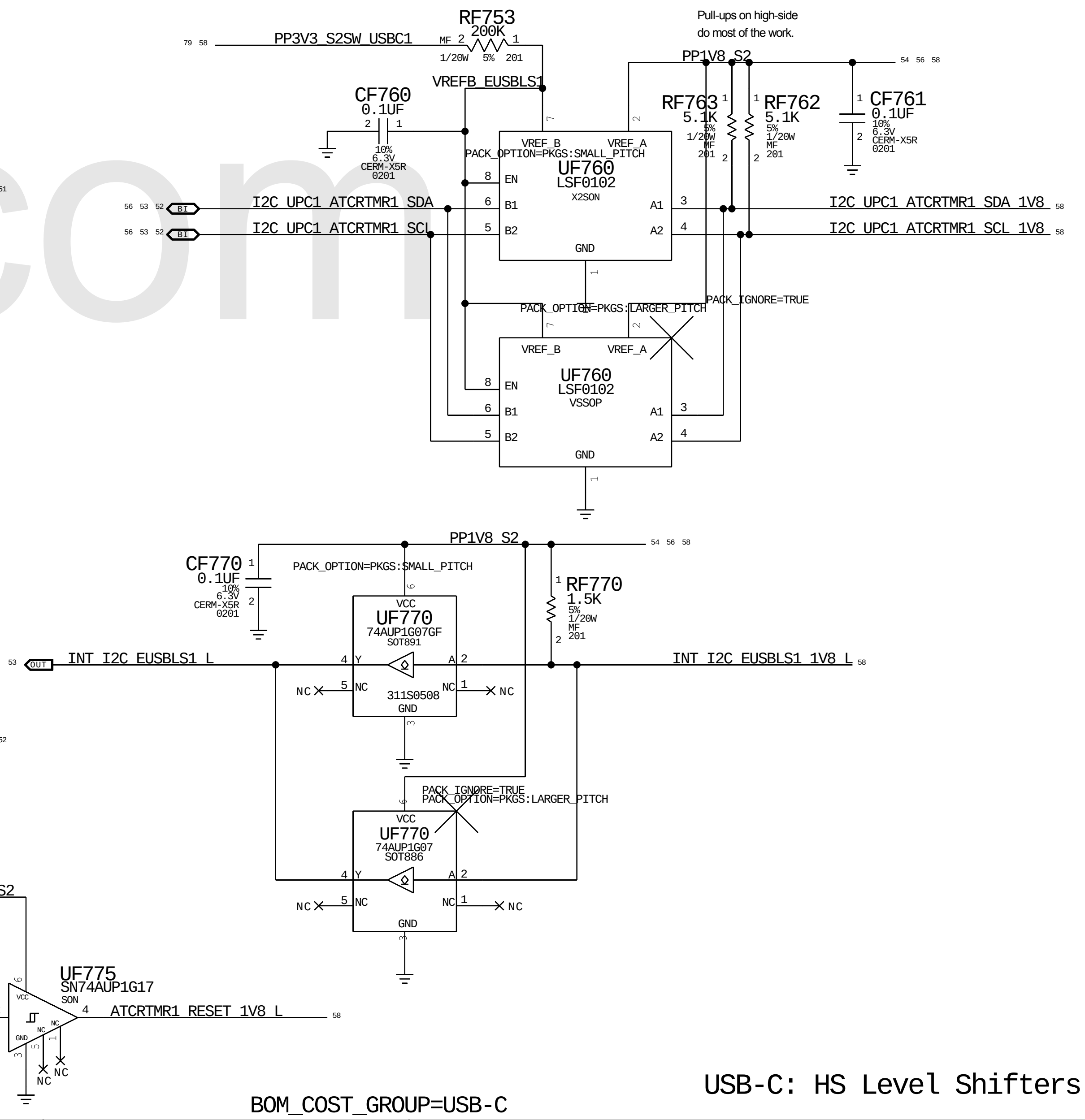
PARROT 0 I2C/RESET LEVEL SHIFTERS



TBT LS RX/TX LEVEL SHIFTERS

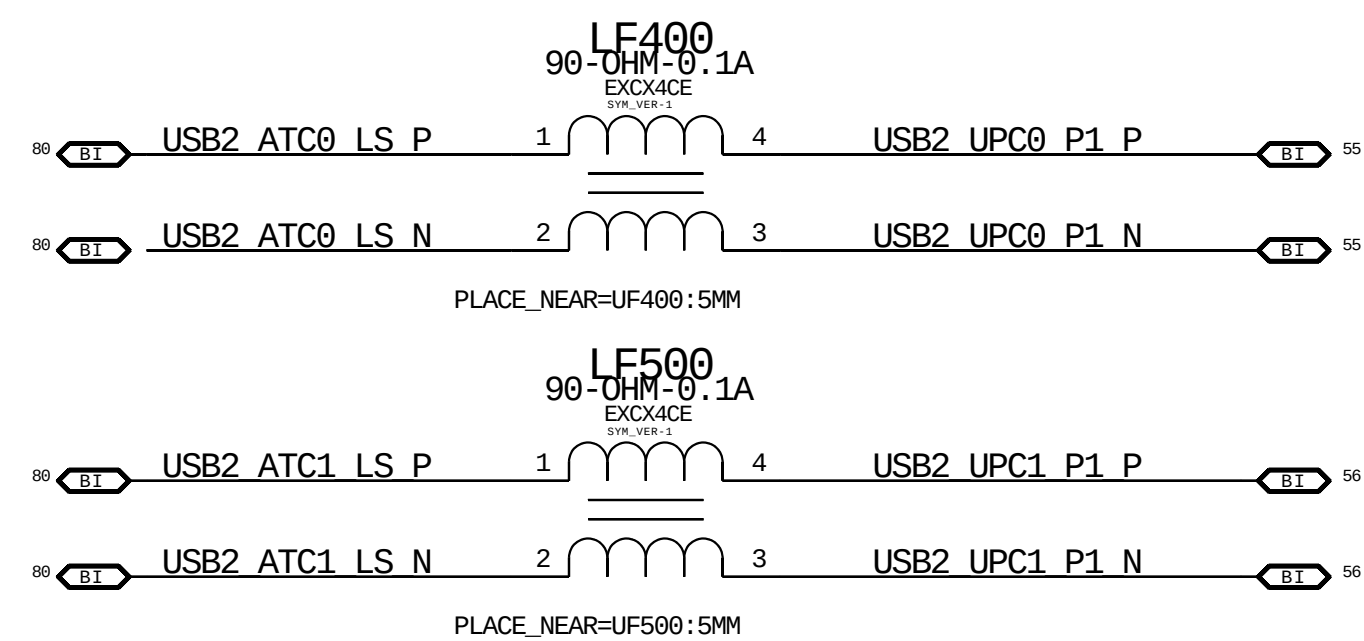
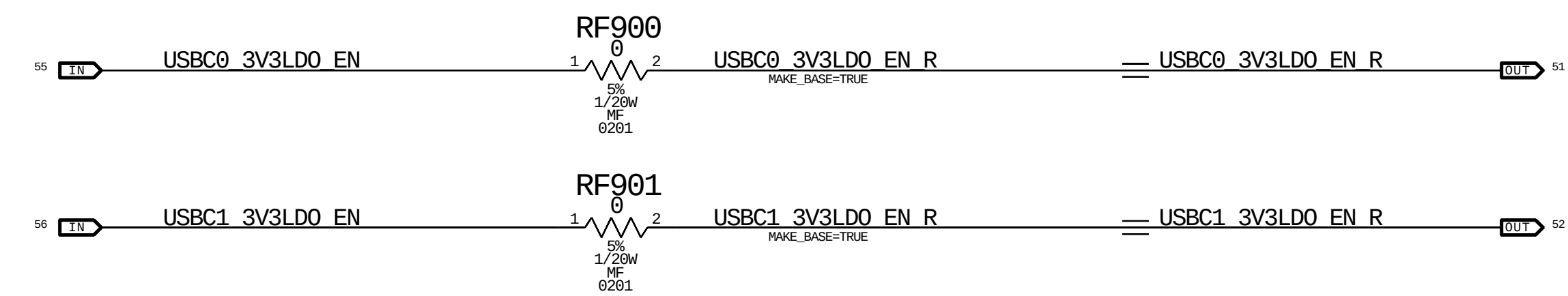


PARROT 1 I2C/RESET LEVEL SHIFTERS

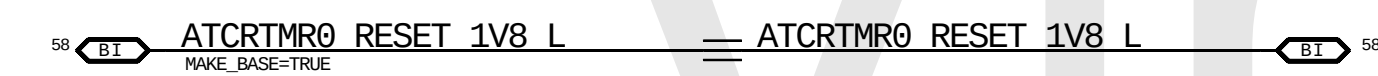


USB-C: HS Level Shifters

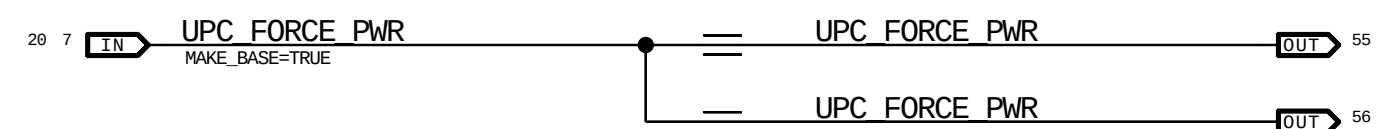
BOM_COST_GROUP=USB-C



Alias Debug Reset signal to ATC0 Debug Level Shifter (UF700)



Tie ACE2 Pin C4 (GPIO6) together and alias to UPC_FORCE_PWR.

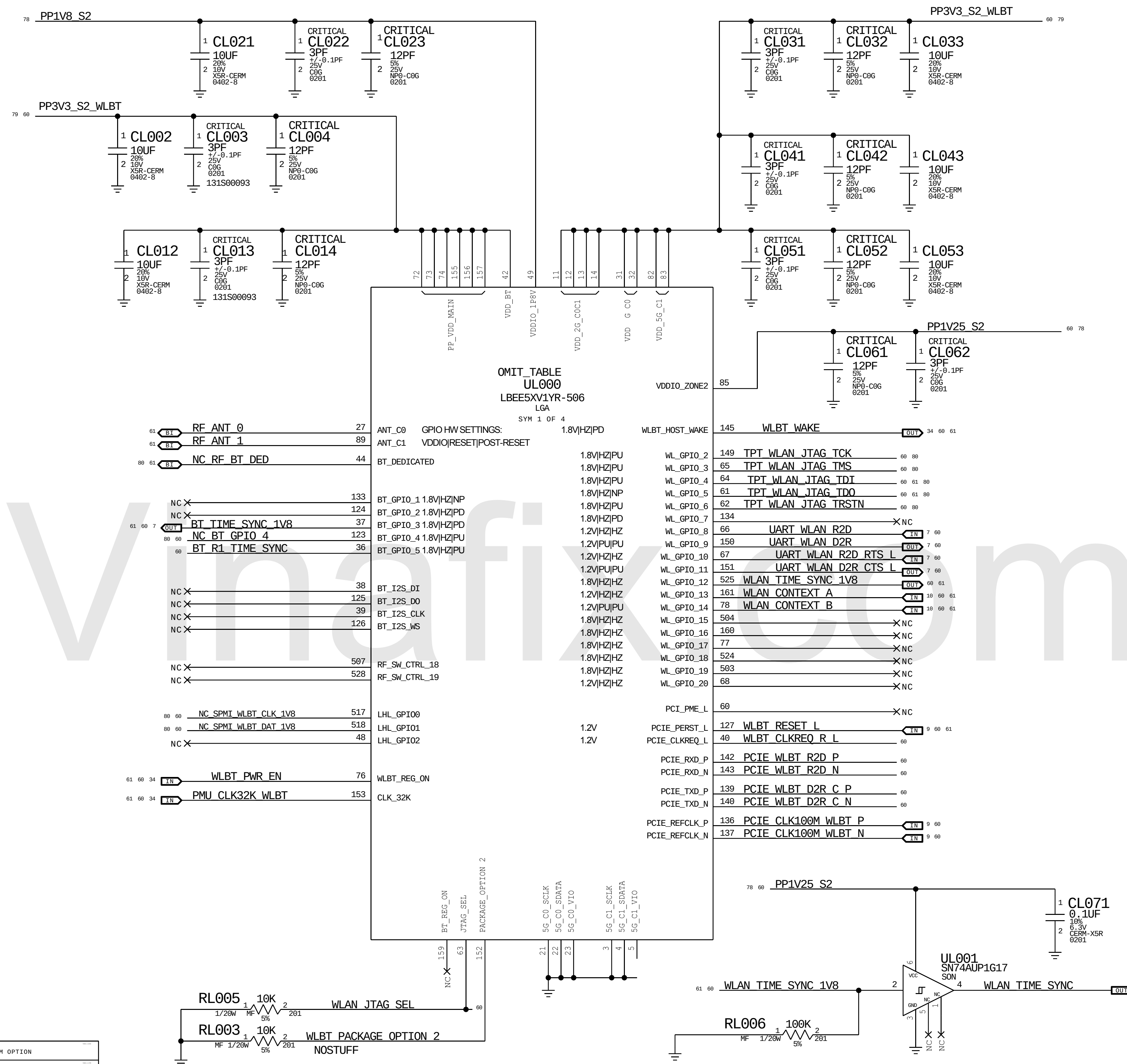


*** OK2INTEGRATE ***

RASPUTIN WIFI/BT MODULE

FOR HOSTINTERFACE TABLES REFER TO:
RDAR://PROBLEM/53187294

FOR DESIGN, DOCUMENTATION,
SYSTEM INTEGRATION QUESTIONS:
RDAR://PROBLEM/44786407

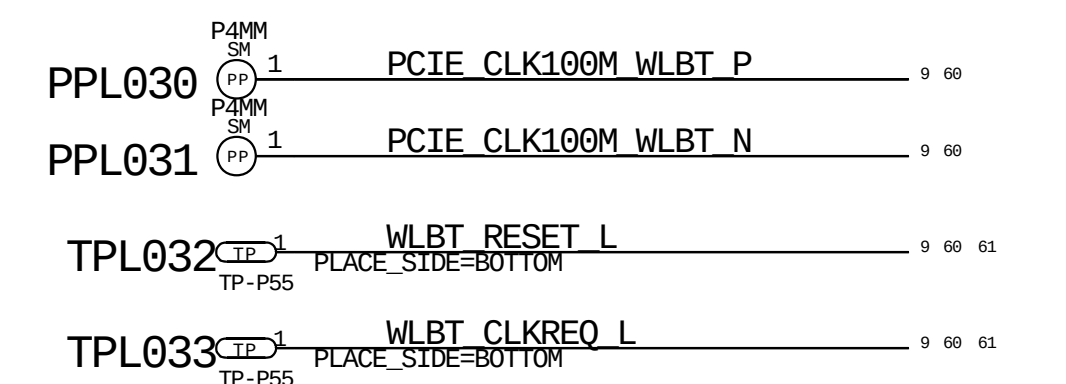
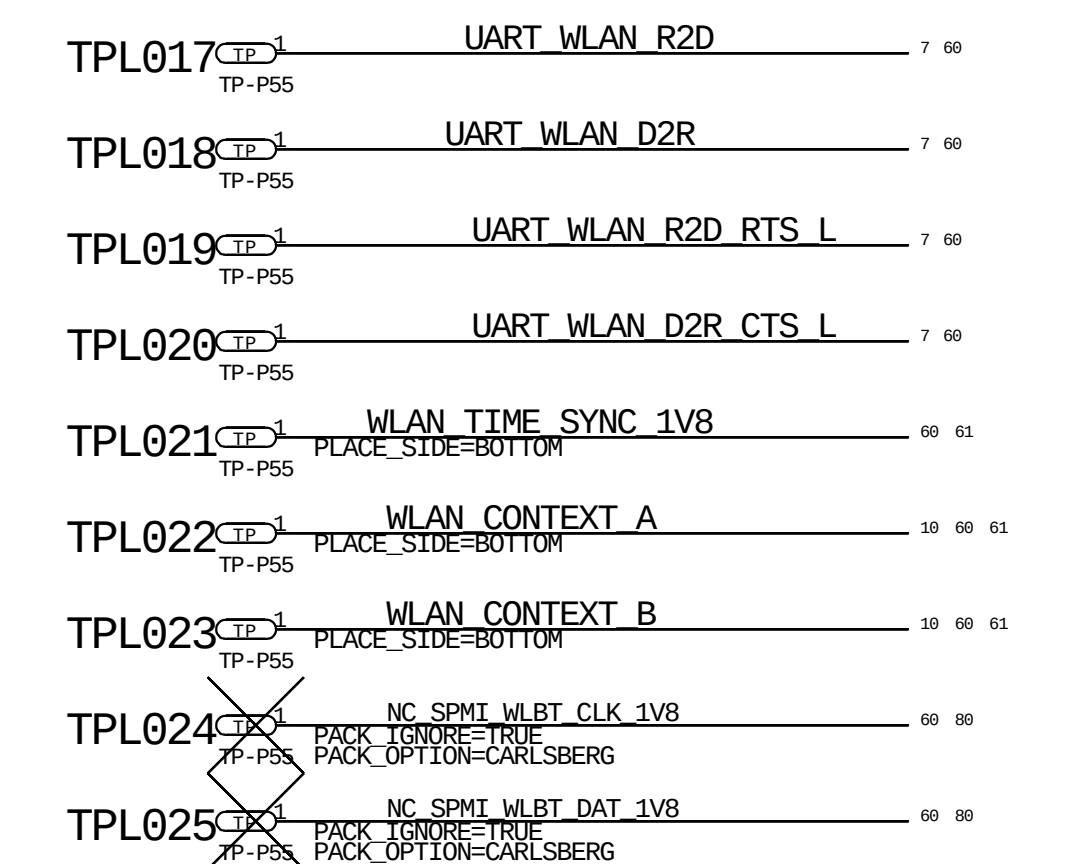
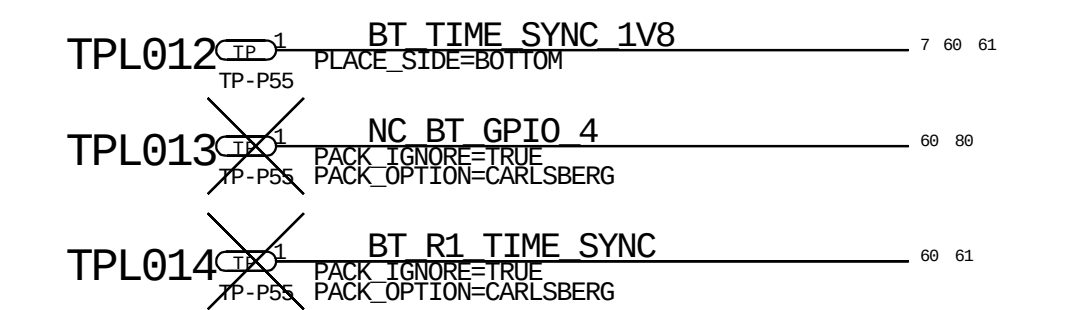
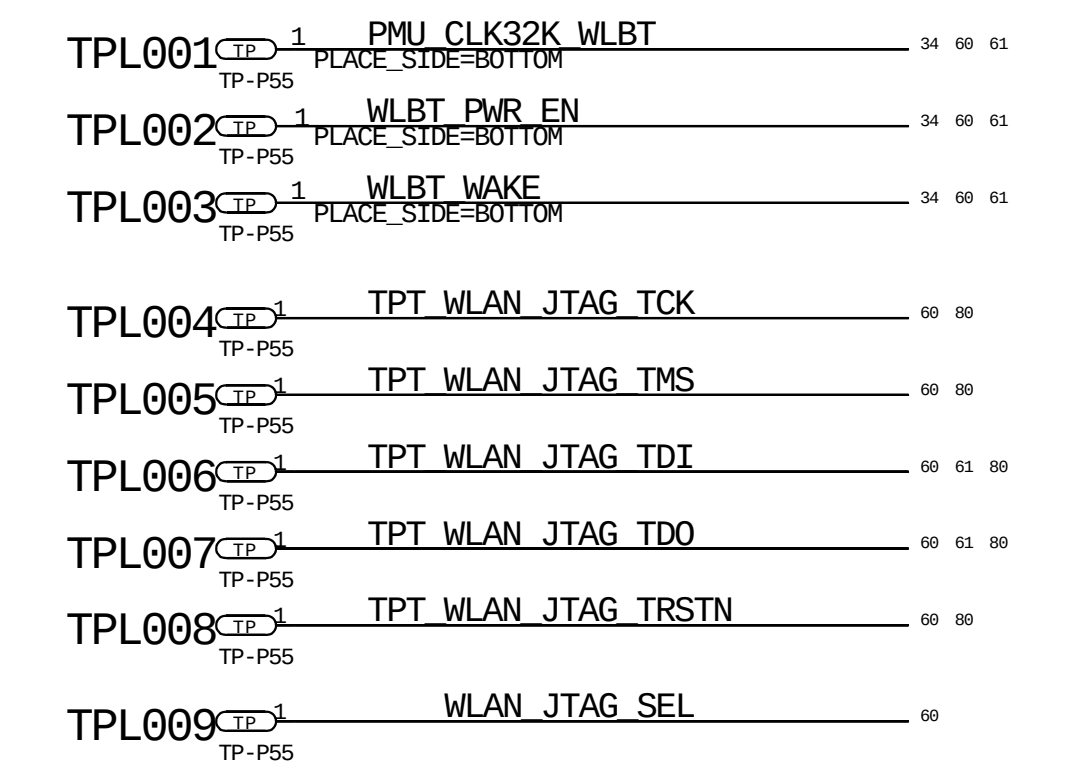
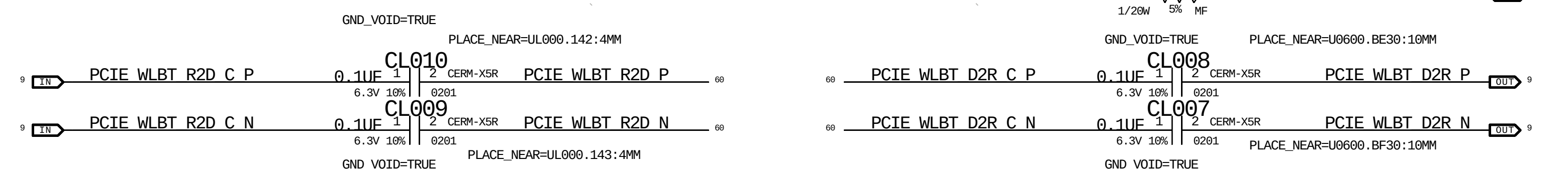


RASPUTIN BOM TABLE:

Part#	Qty	Description	Reference Designator(s)	Critical	BOM Option
339S00763	1	MODULE, MAIN BT, RASPUTIN, E50.11, M, LEAS40	UL000	CRITICAL	

RASPUTIN ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00758	339S00763	ANY	UL000	RASPUTIN USI ES6.5

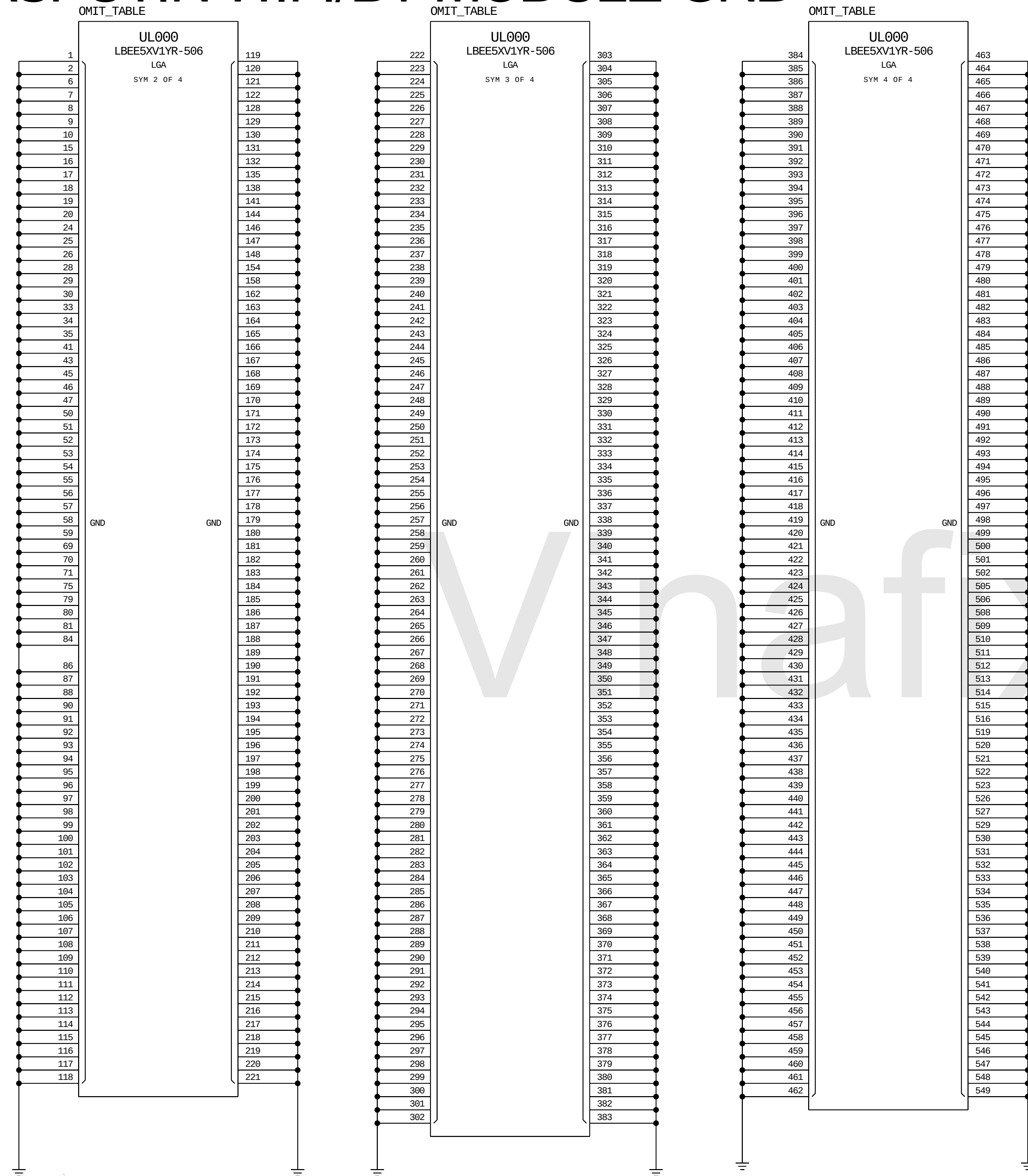


WIFI/BT: MODULE

BOM_COST_GROUP=WIRELESS

*** OK2INTEGRATE ***

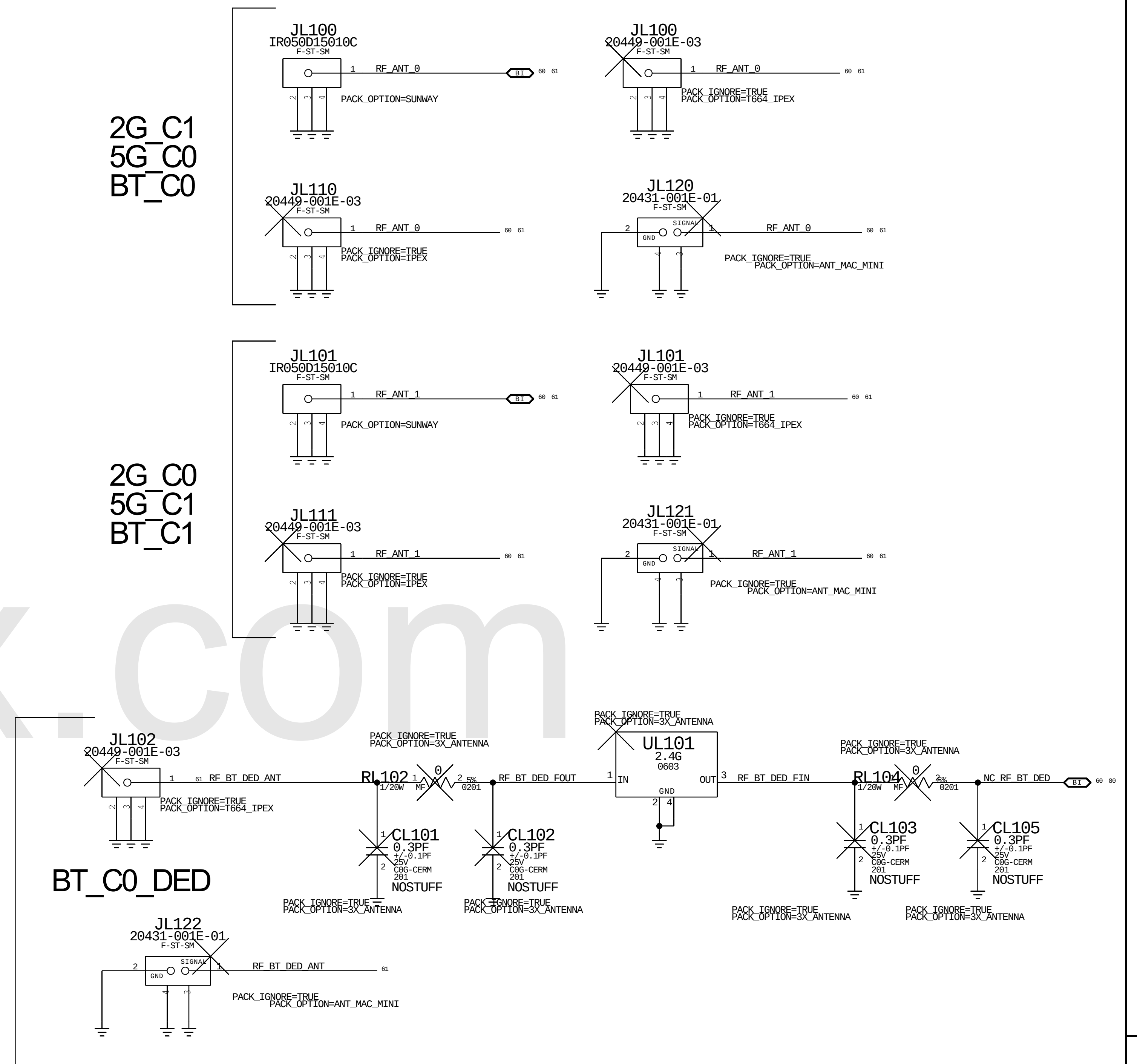
RASPUTIN WIFI/BT MODULE GND



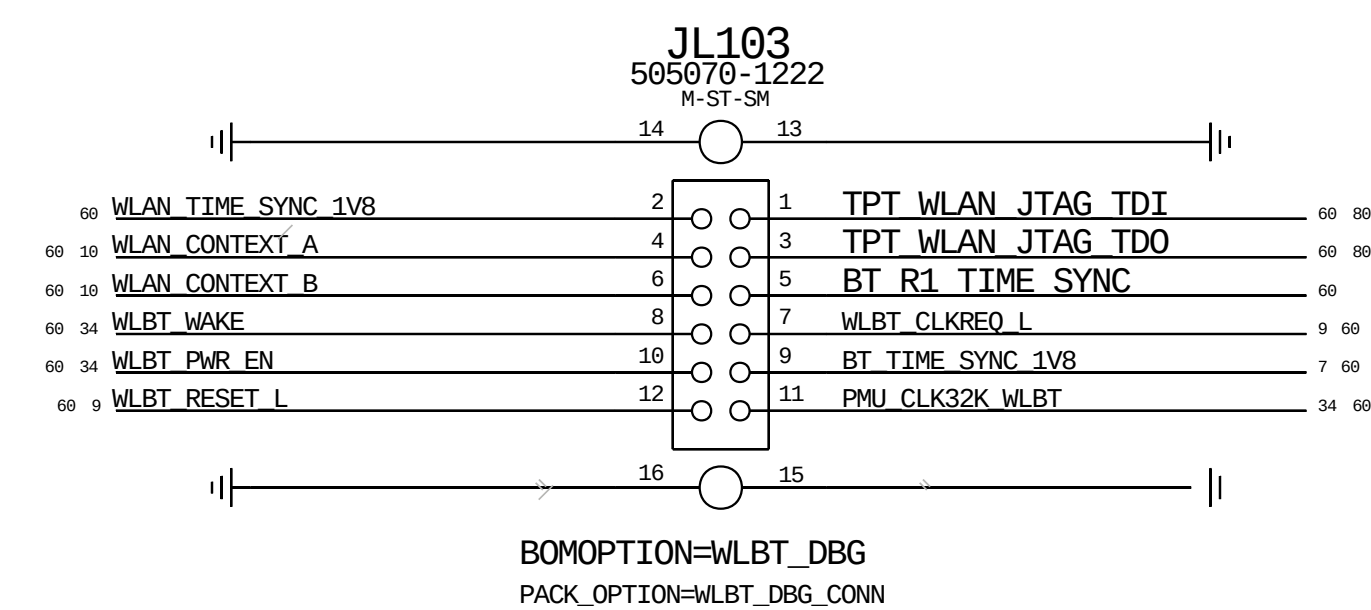
ANTENNA CONNECTORS

2G_C1
5G_C0
BT_C0

2G_C0
5G_C1
BT_C1



WLBT DEBUG CONNECTOR



WIFI/BT: ANTENNA and GND

NAND0 S5E0



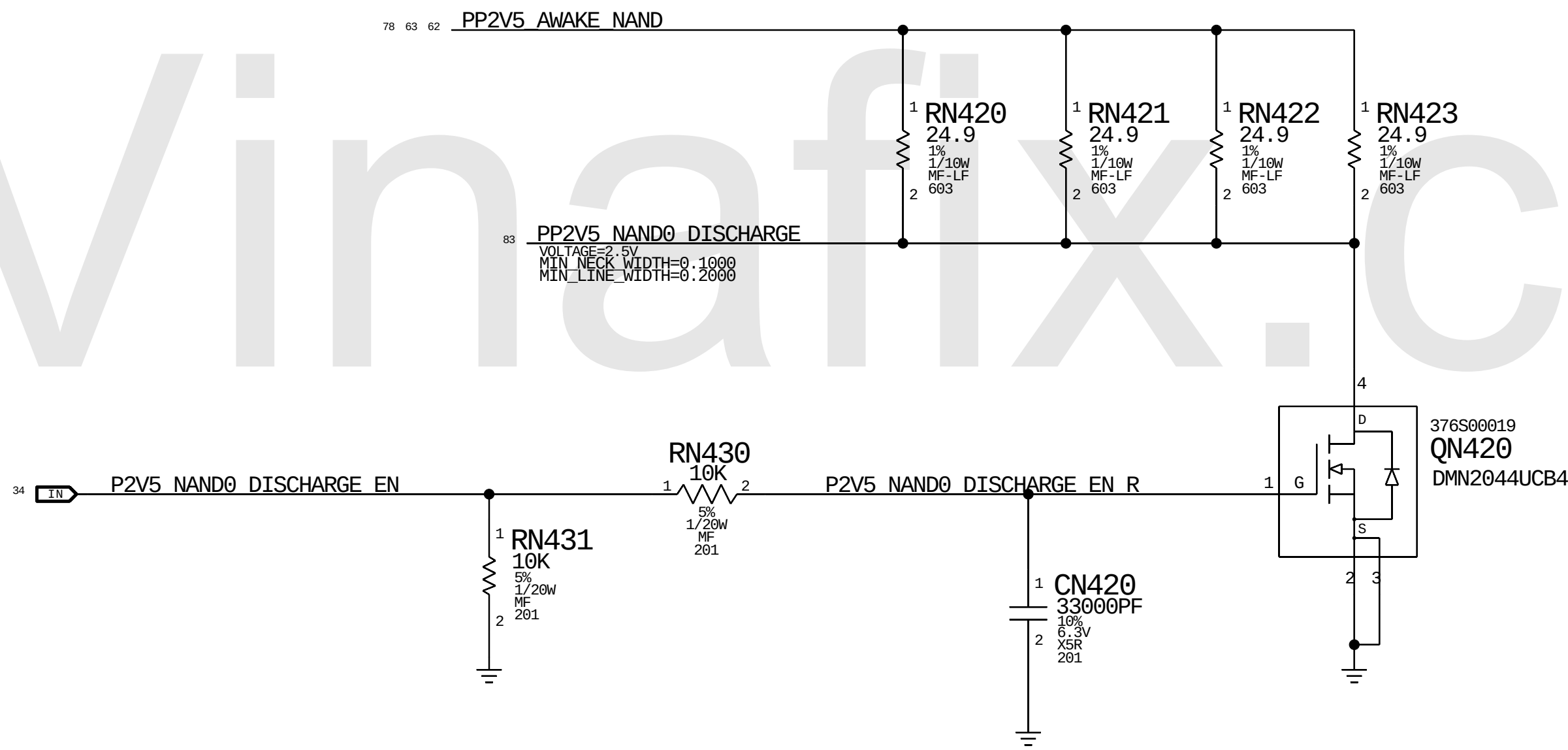
NAND0 S5E1



Vinafix.com

OK2INTEGRATE

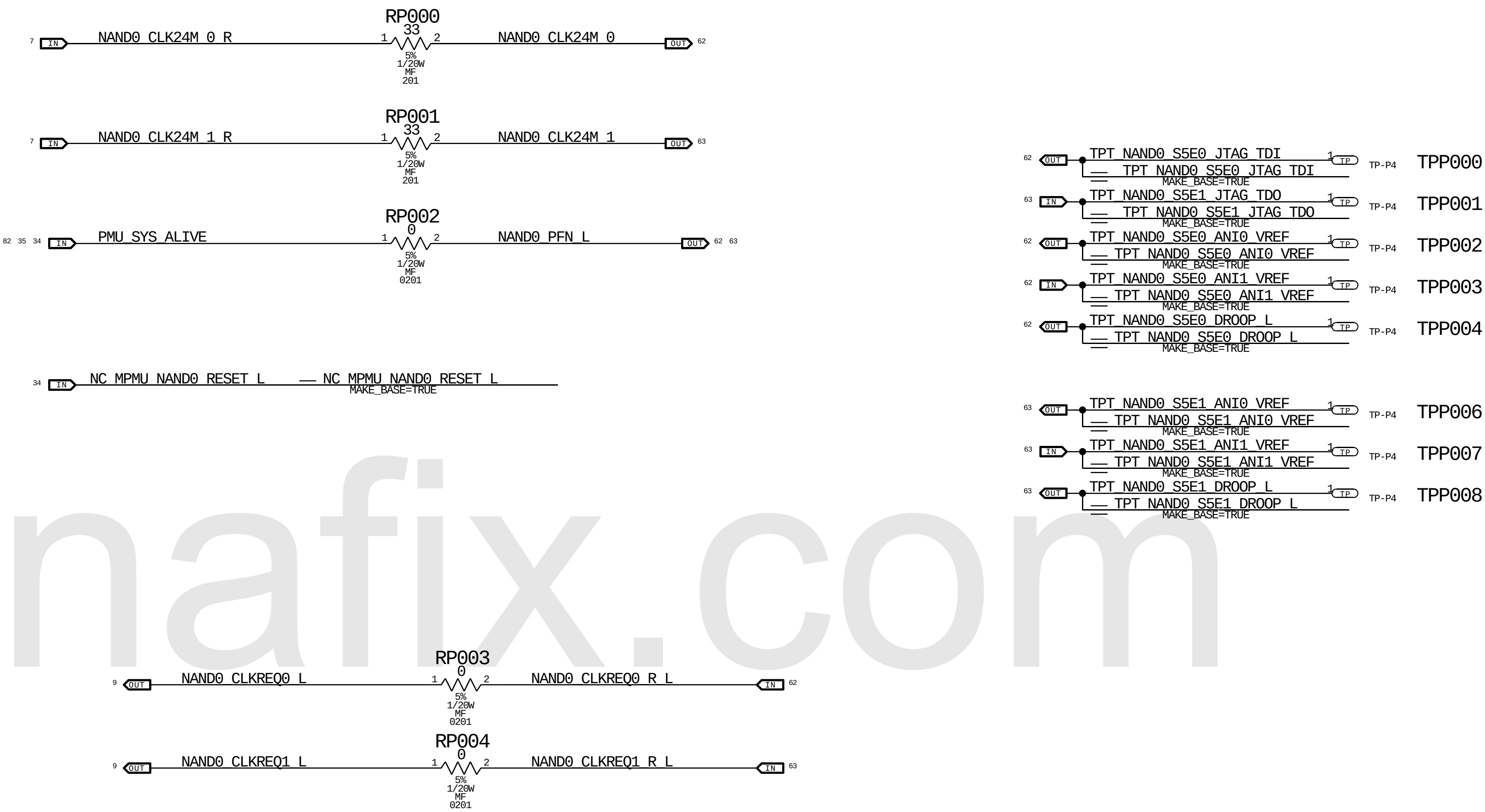
THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



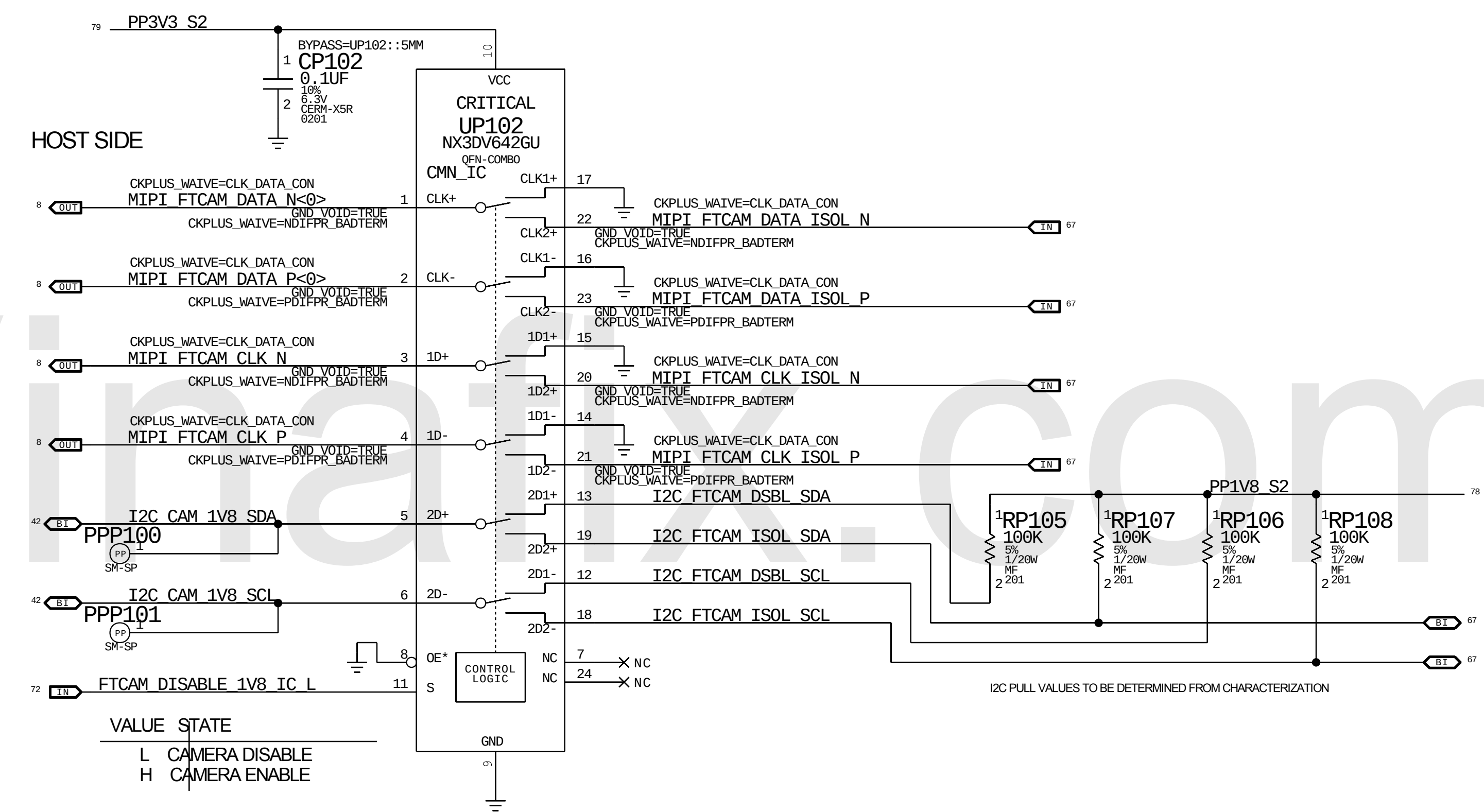
STORAGE: NON OCARINA SUPPORT

SSD 24M CLOCK TERMINATIONS

TOPOLOGY TBD



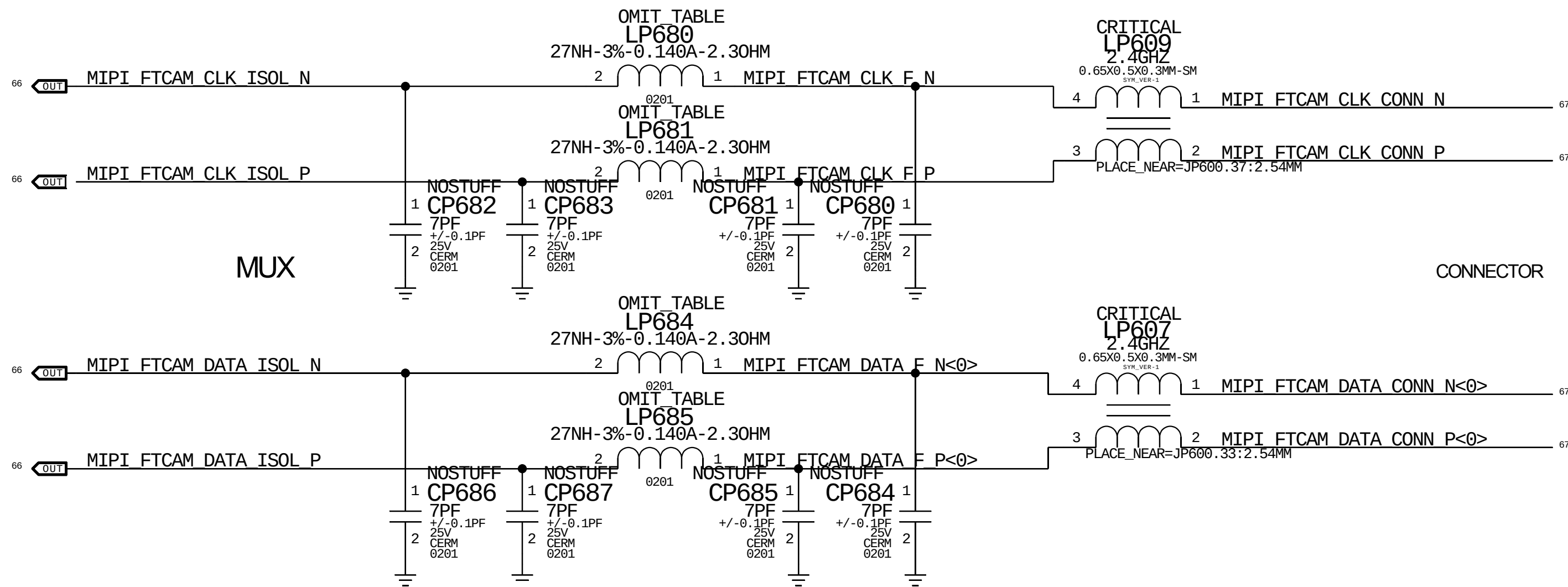
CAMERA SECURE DISABLE



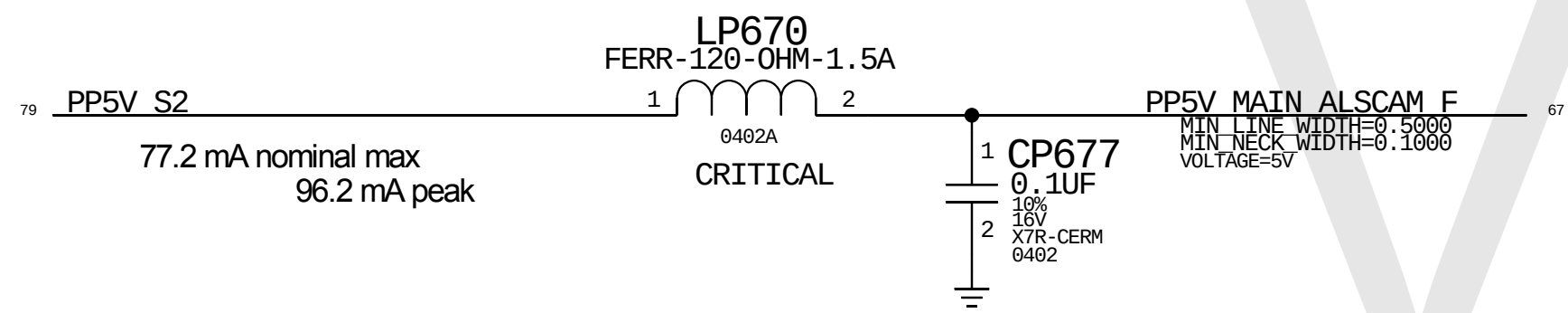
LCD PANEL INTERFACE (eDP) + Camera (MIPI)

A MIPI Clock and Data

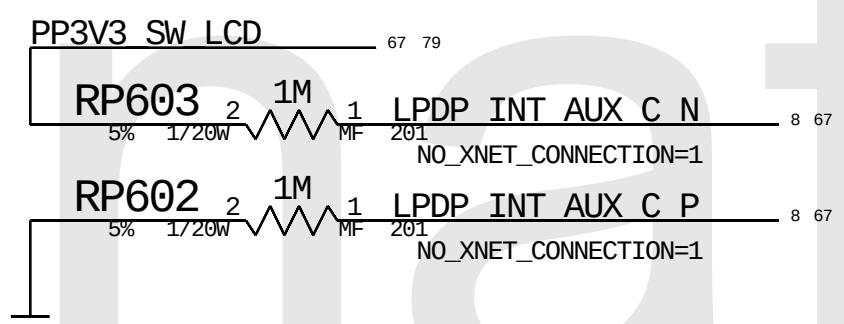
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11750201	4	RES, MF, 1A MAX, 0.9 OHM, 5%, 0201, BLACK	LP680, LP681, LP684, LP685		



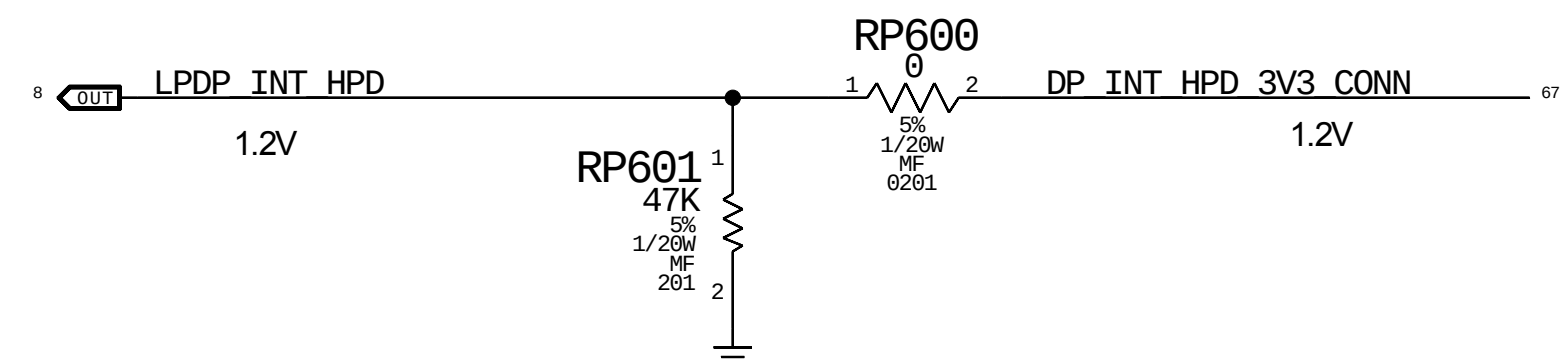
B ALS & Camera 5V Filter



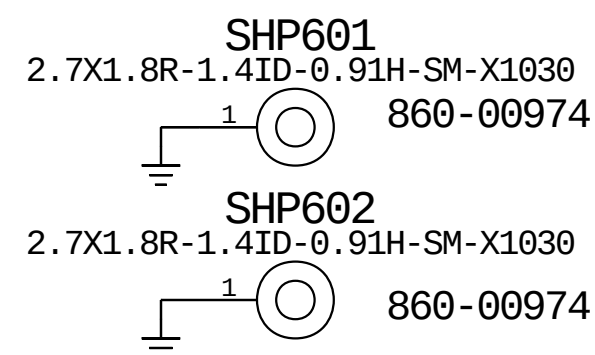
C LCD Panel AUX Straps



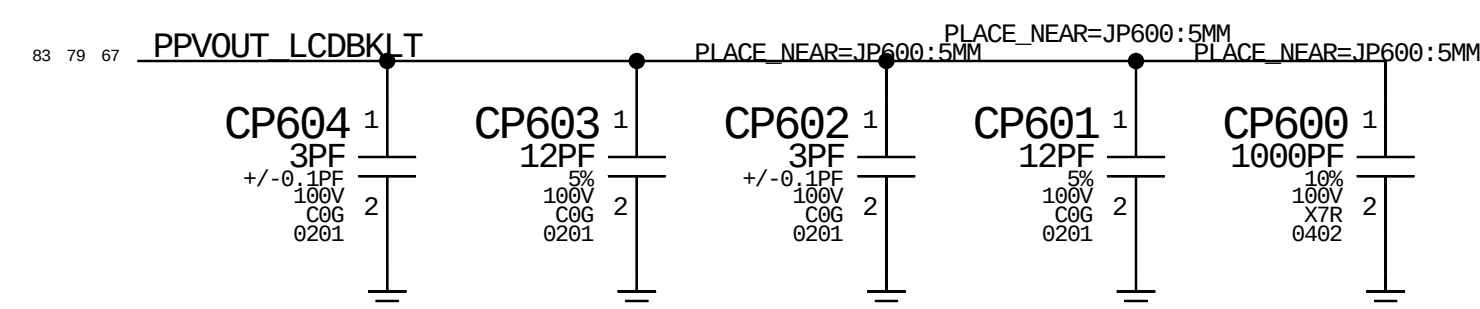
D TCON HPD Voltage Divider



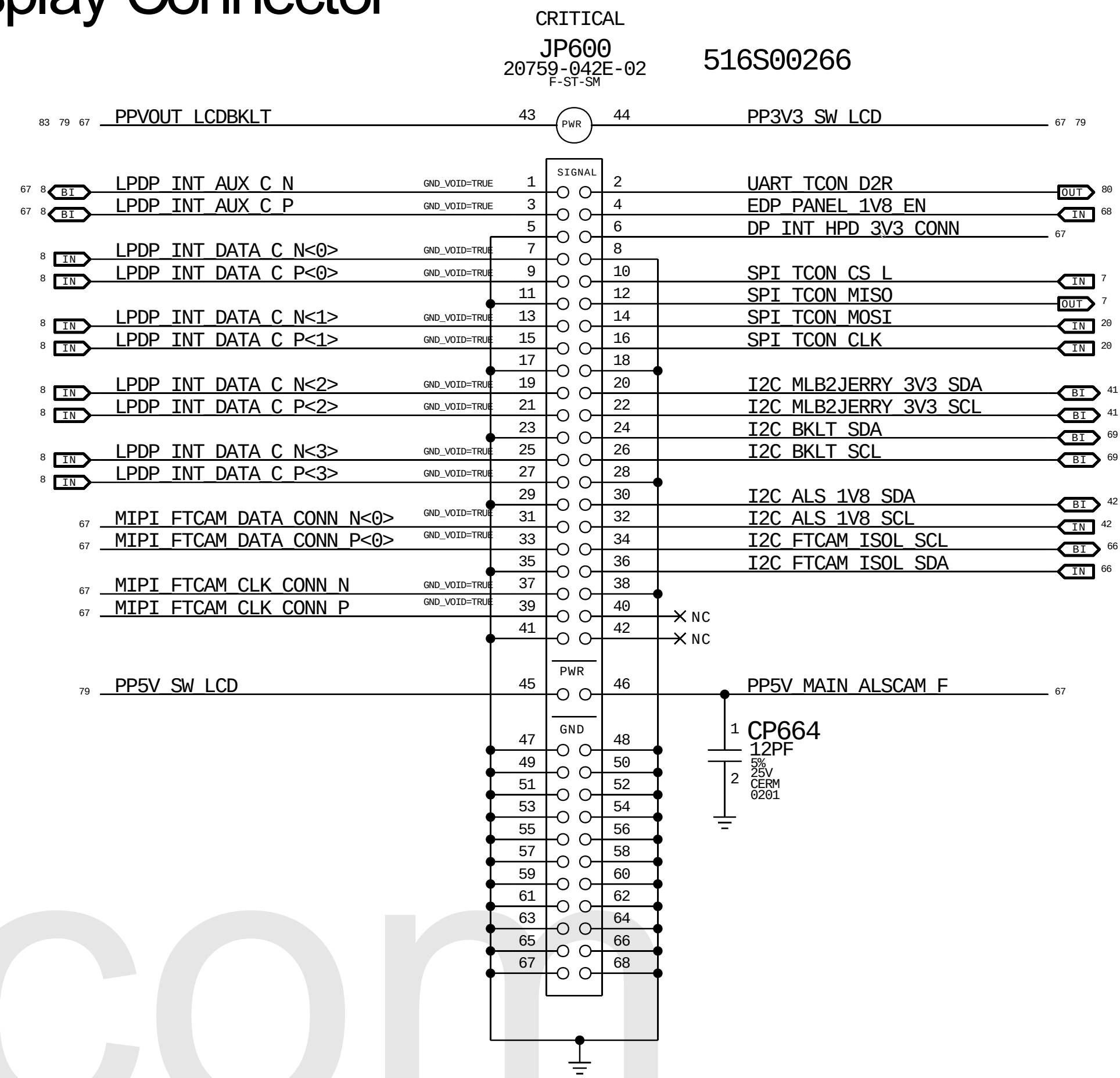
E Cowling Bosses



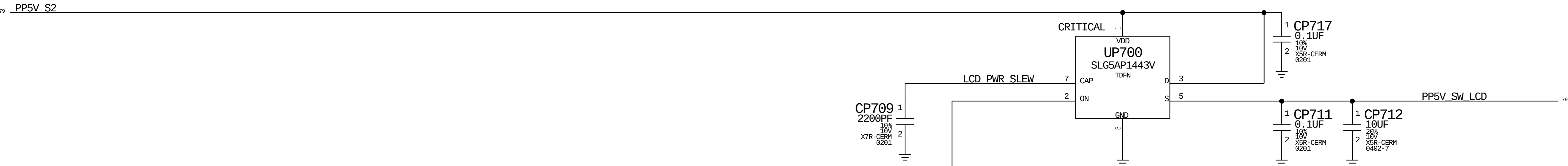
F Backlight Desense Capacitors



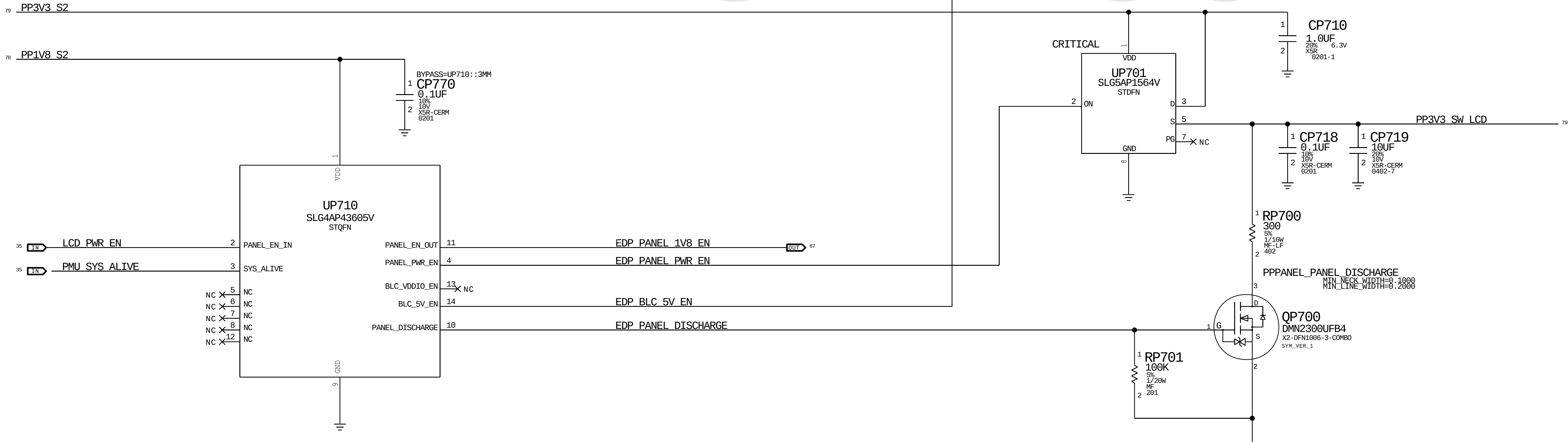
G eDP Display Connector



*** OK2INTEGRATE ***



CONSULT YOUR DISPLAY DRI FOR DETAILS
GENERAL GUIDELINE IS
3V3 FOR 2020 SYSTEMS
3V8 FOR 2021 SYSTEMS



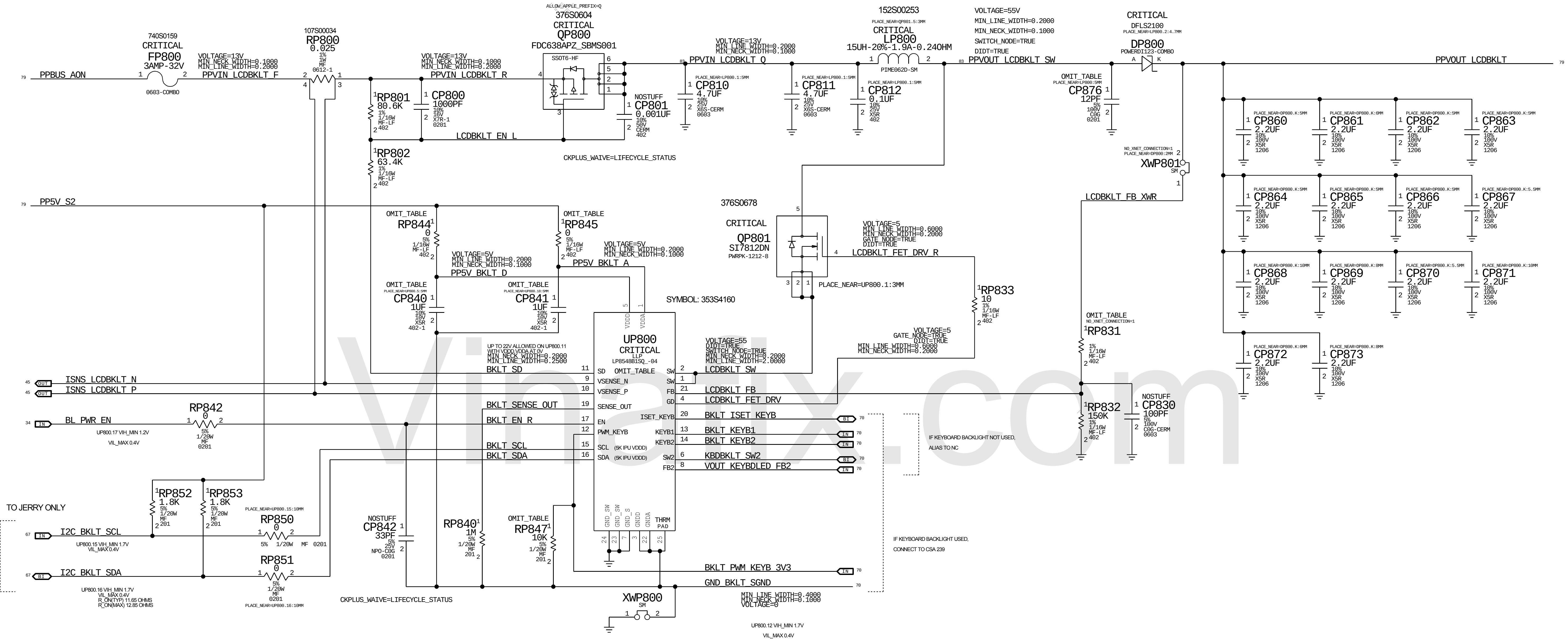
DISPLAY POWER SEQUENCER

BOM_COST_GROUP=DISPLAY

*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER

371S00077 (COMBO) FOOTPRINT IN LAYOUT



BEN IC VERSION TO MATCH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC, LP8488B-04, DC/DC, CTR, BOOST, 0.24	UP800		BLC_BEN_IC:V4
353S02256	1	IC, LP8488B-07, DC/DC, BOOST, CTR, 0.24	UP800		BLC_BEN_IC:V7

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP, C0G, 12PF, 5%, 180V, 0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (J132, J213)
100K IF KEYBOARD PWM INPUT IS PRESENT (J152)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0007	1	RES, MF, 1/20W, 10K OHM, 5%, 0201, SPD	RP847		BLC_KBD_BOOST_USED:NO
118S0014	1	RES, MF, 1/20W, 10K OHM, 5%, 0201, SPD	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEADS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0339	1	RES, MTL FILM, 1/10W, 18.2K, 1%, 0402, SM, LF	RP831		BLC_LEDS_PER_STRING:16
114S0359	1	RES, MTL FILM, 1/10W, 28.7K, 1%, 0402, SM, LF	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V R/C FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION. AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDD5 & VDDA, SEE <RDR-50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES, MTL FILM, 0 OHM, 1A MAX, 0402, SPD	RP844, RP845		BLC_5V_SERIES:0_OHM
114S0023	2	RES, MTL FILM, 1/10W, 10 OHM, 1%, 0402, SPD, LF	RP844, RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP, CER, X5R, 1UF, 18V, 10%, 0402	CP840, CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP, CER, X5R, 4.7UF, 25V, 10%, 0402	CP840, CP841		BLC_5V_CAP:4P7_UF

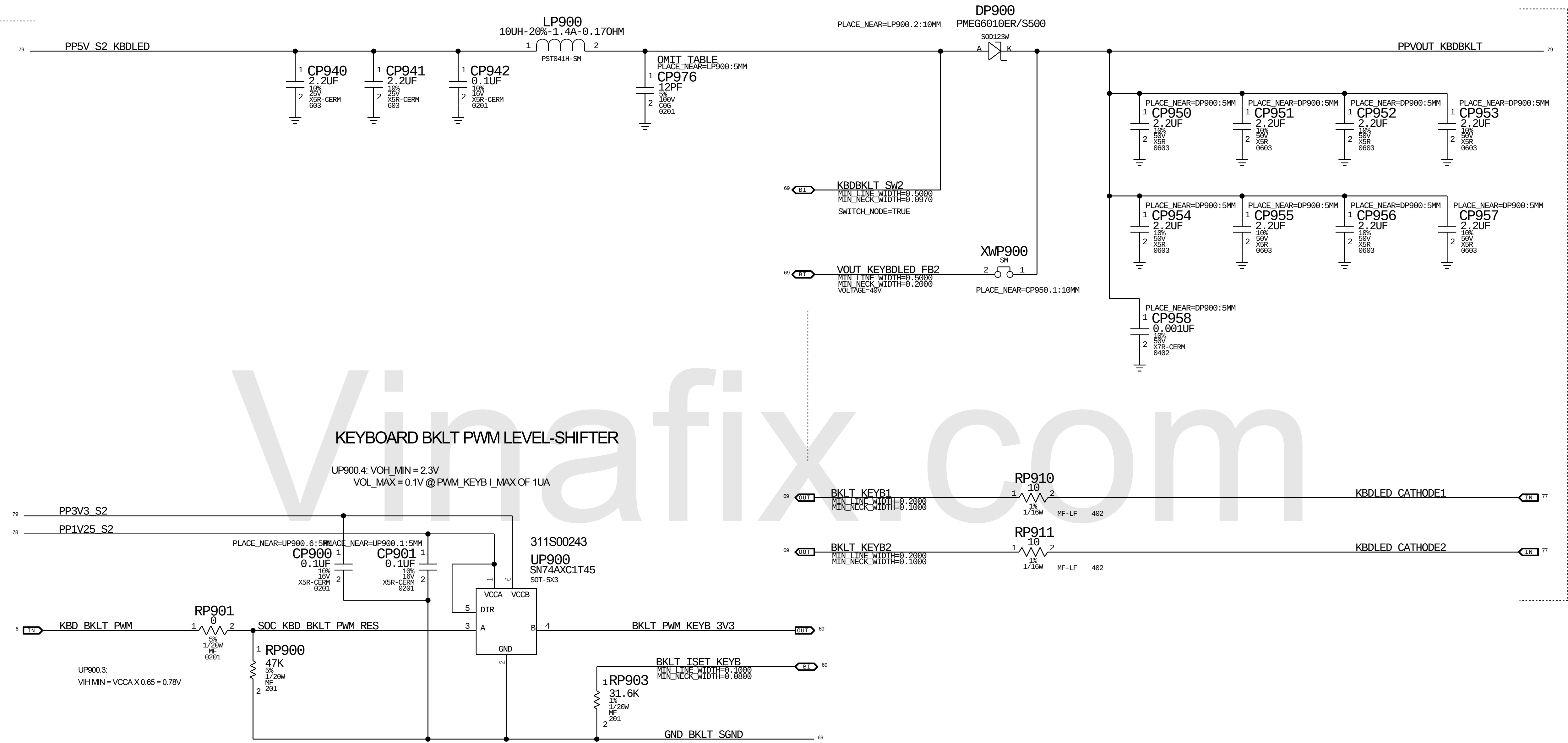
BOM_COST_GROUP=DISPLAY

BEN: CONTROLLER

*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

THIS PAGE IS ONLY TO BE INCLUDED IF THE KEYBOARD BACKLIGHT
IS CONTROLLED BY THE BEN ON PAGE 238



OFF=PAGE SIGNALS ON THIS VERTICAL LINE CONNECT TO BEN UP800
ON PAGE 238

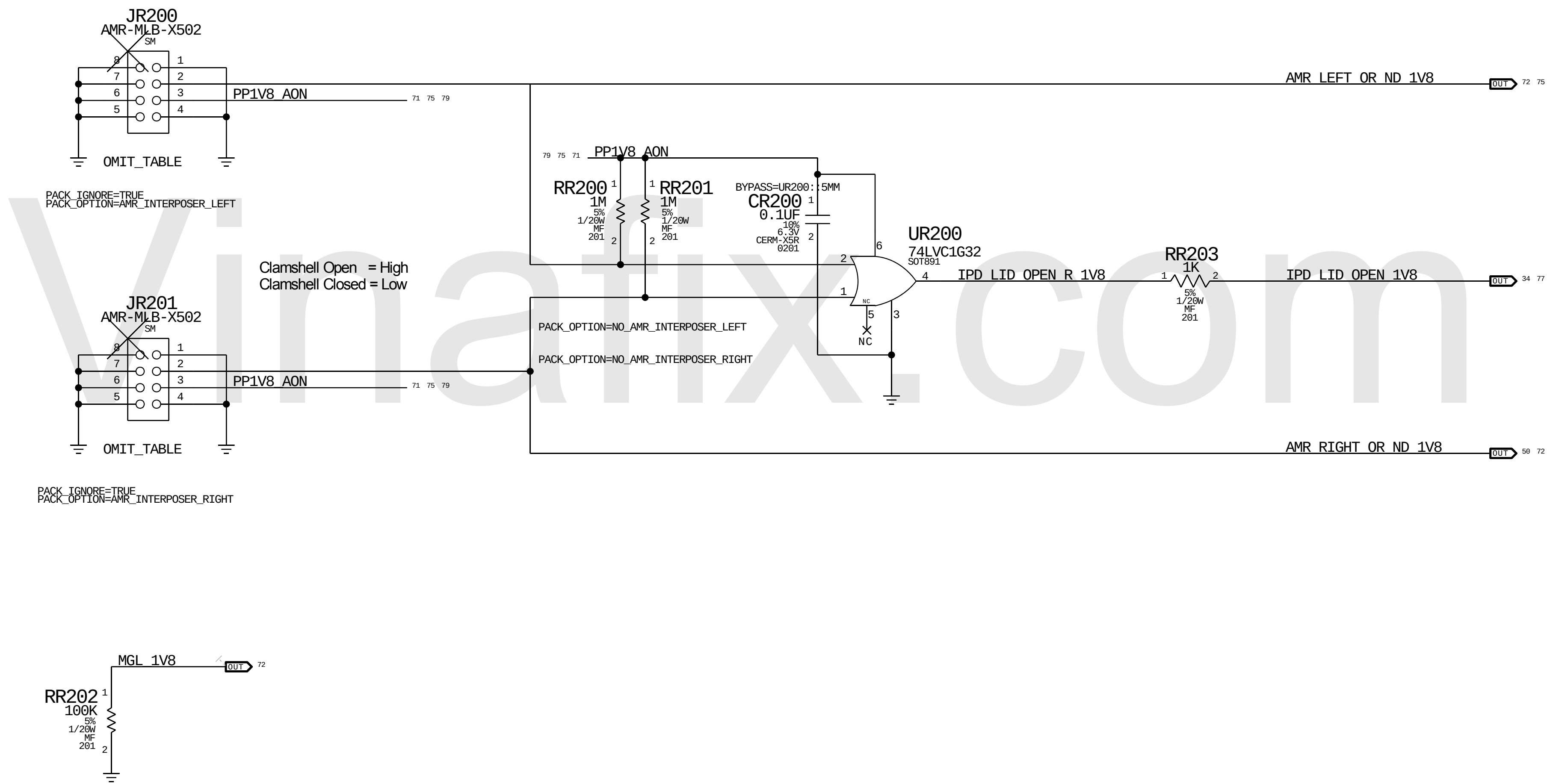
KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM_OPTION
131S00141	1	CAP, C0G, 12PF, 5%, 106V, 0201	CP976		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

BEN: KEYBOARD

Lid Detect Sensors



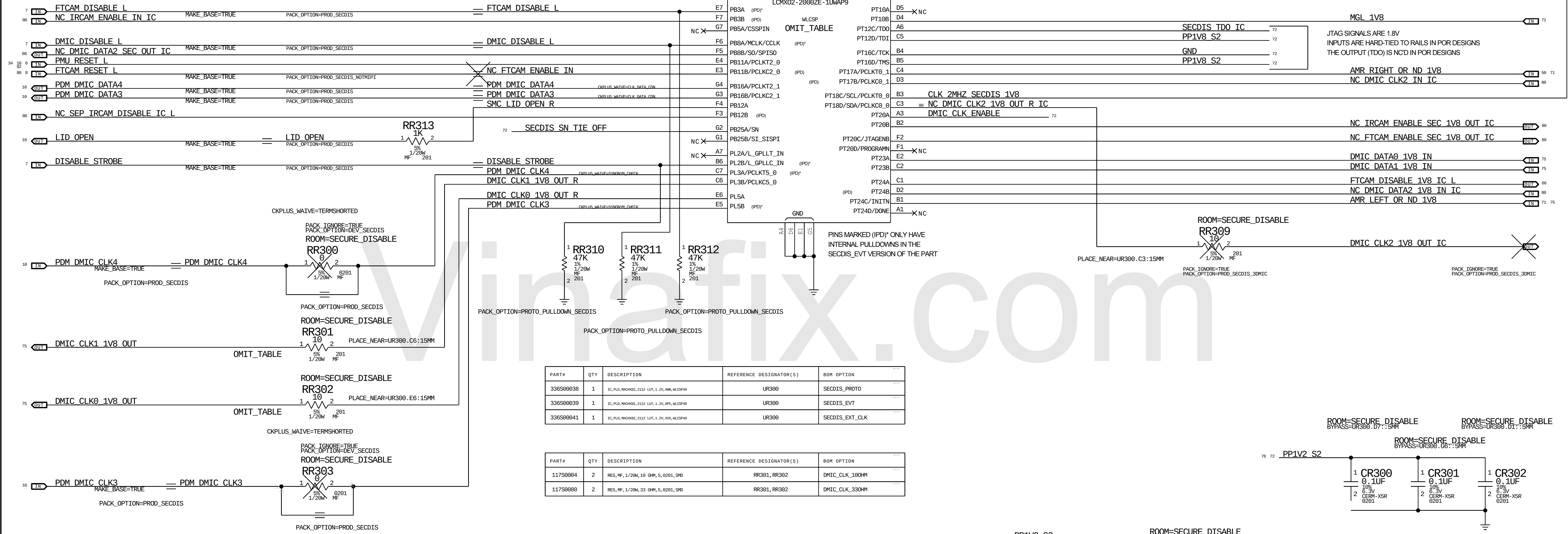
*** OK2INTEGRATE ***

UNLESS 1V8 IS NOTED, SIGNALS ARE 1.2V

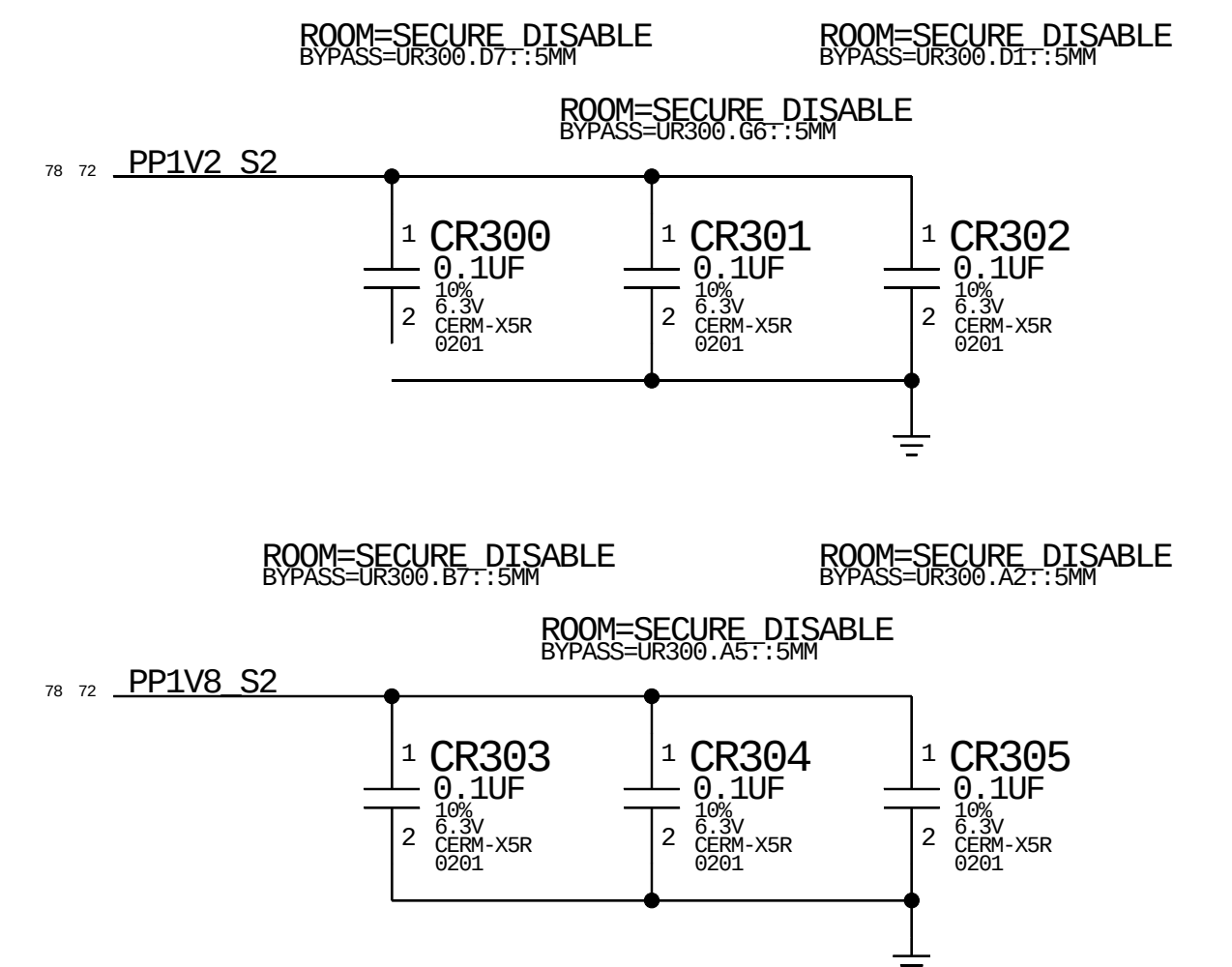
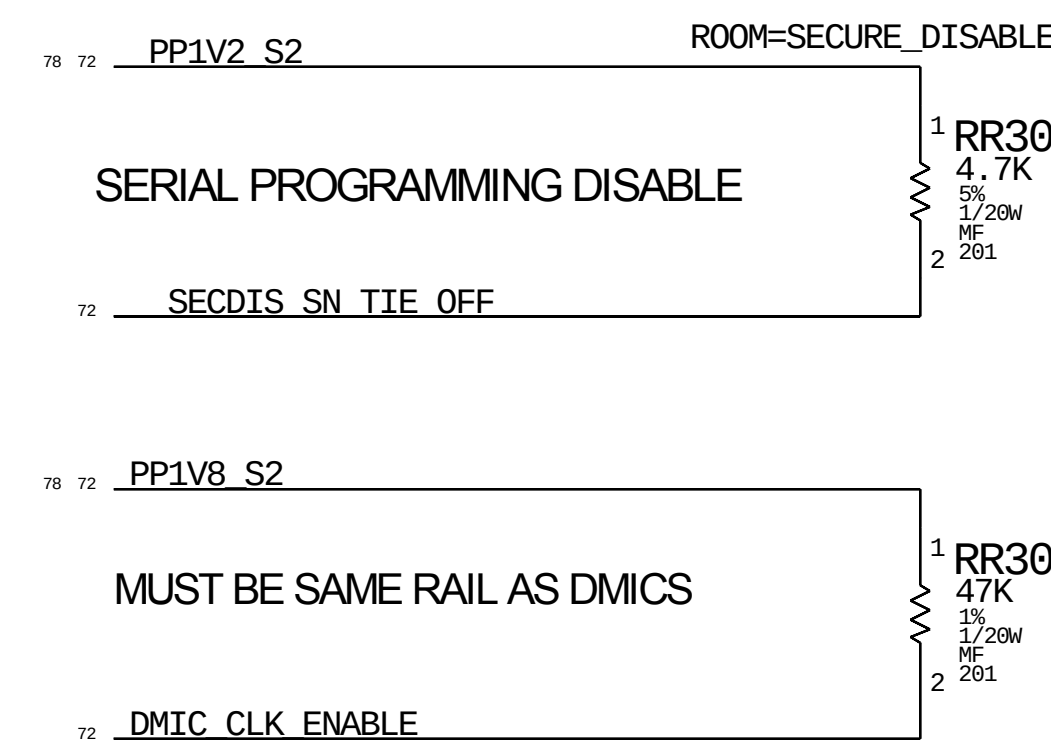
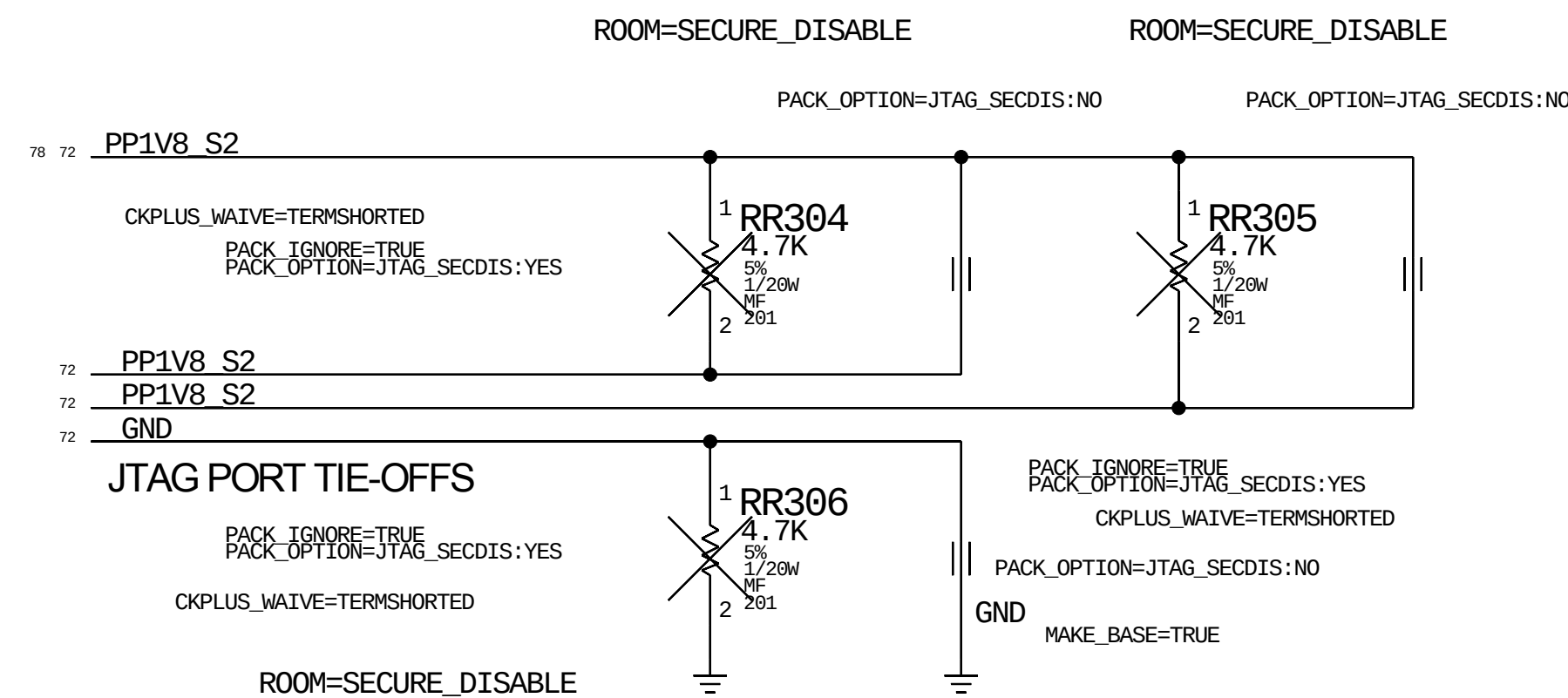
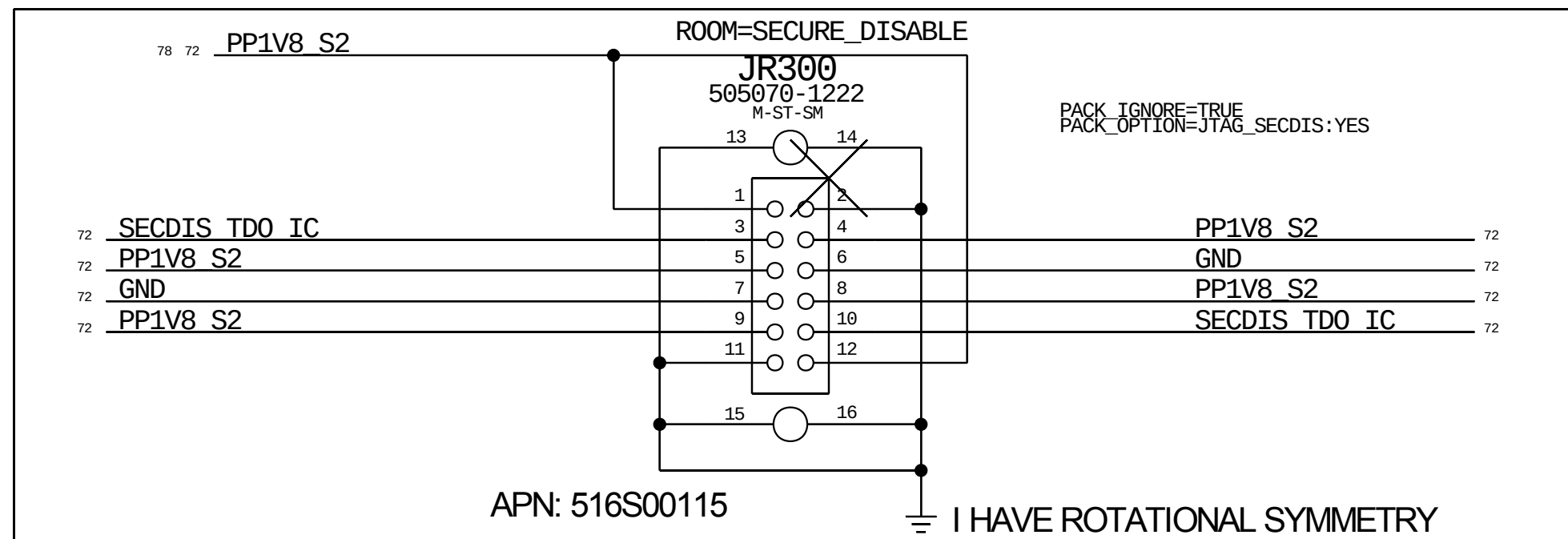
CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	0.8MA	33MA
1.8 S2	0.8MA	14MA

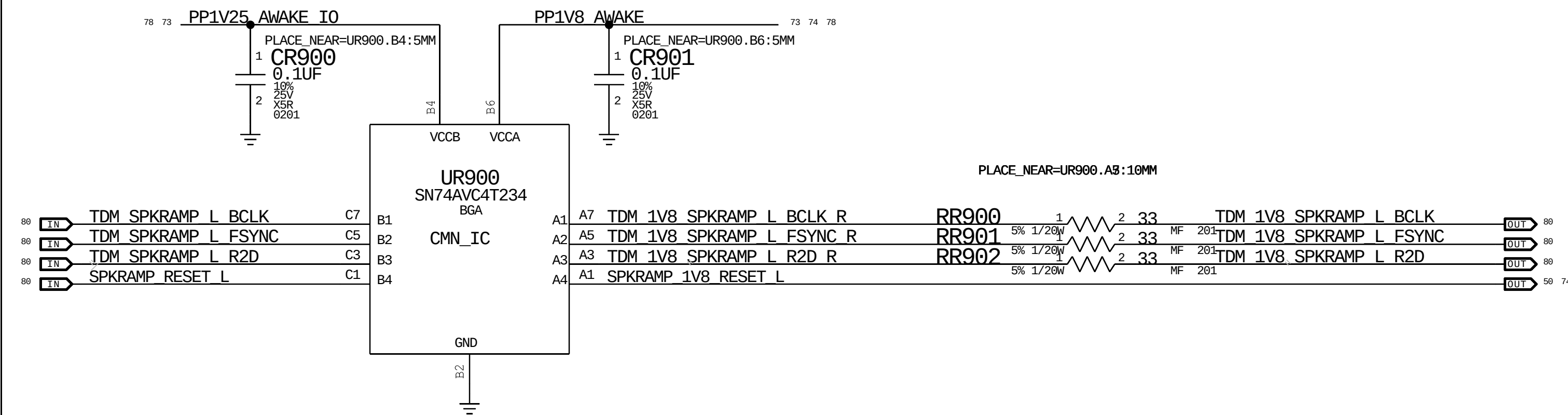
SUPER IMPORTANT PACK OPTIONS:
NOTES ARE ON CSA 2 OF THE REFERENCE DESIGN
READ, LEARN, IMPLEMENT



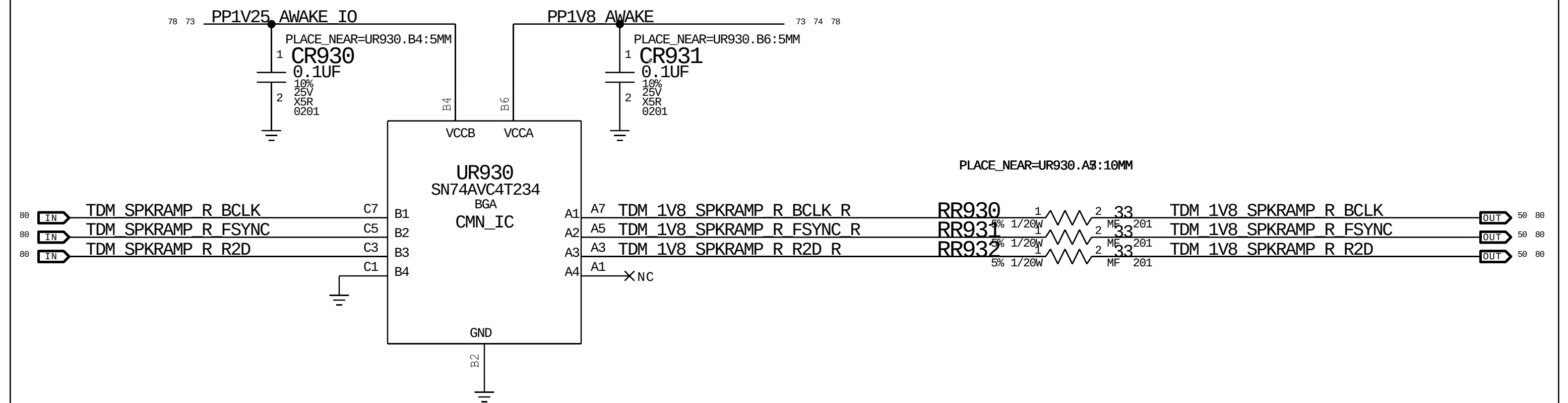
JTAG FOR DEV & PROTO0 BOARDS ONLY



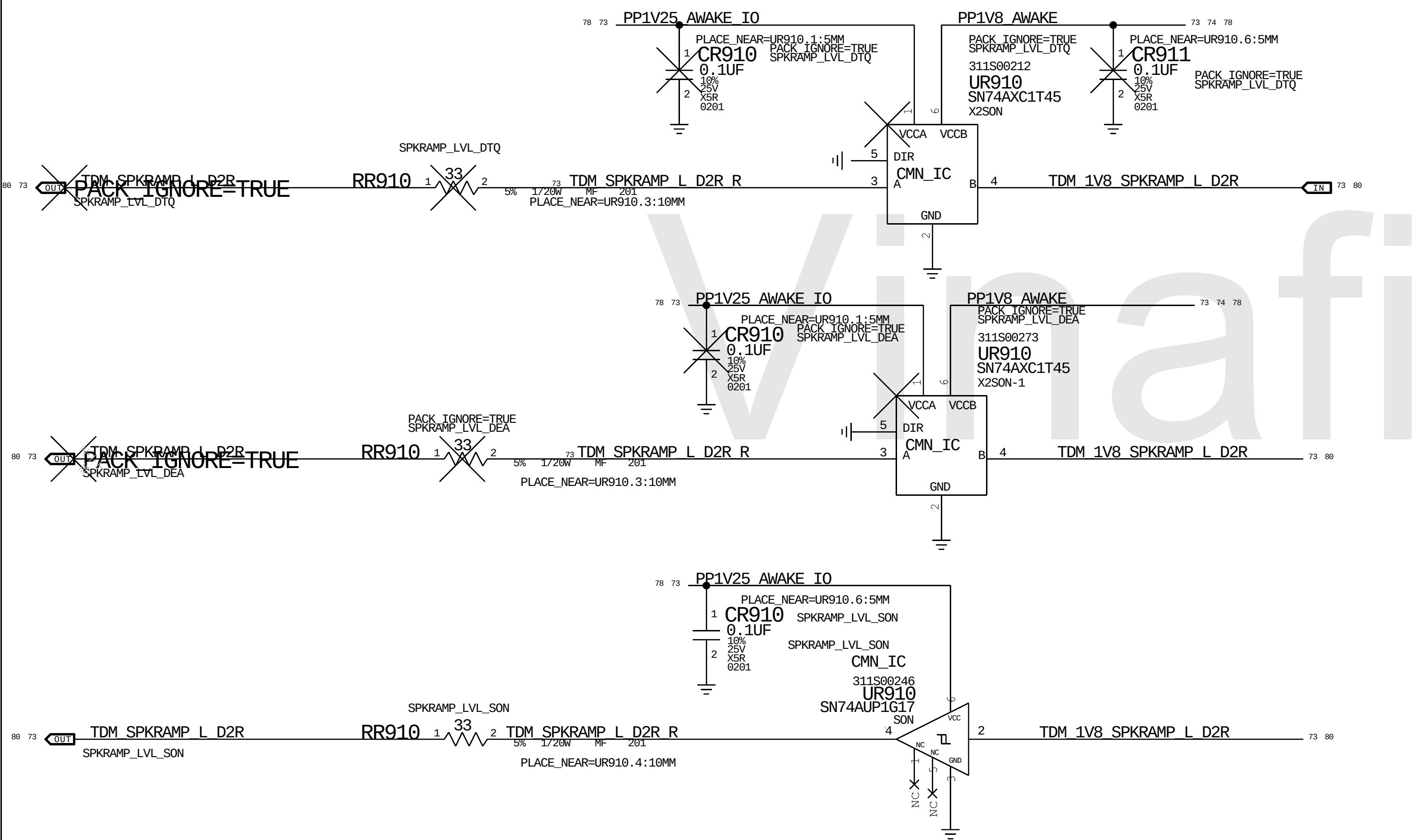
A Left Speaker Amplifier TDM Level Translator



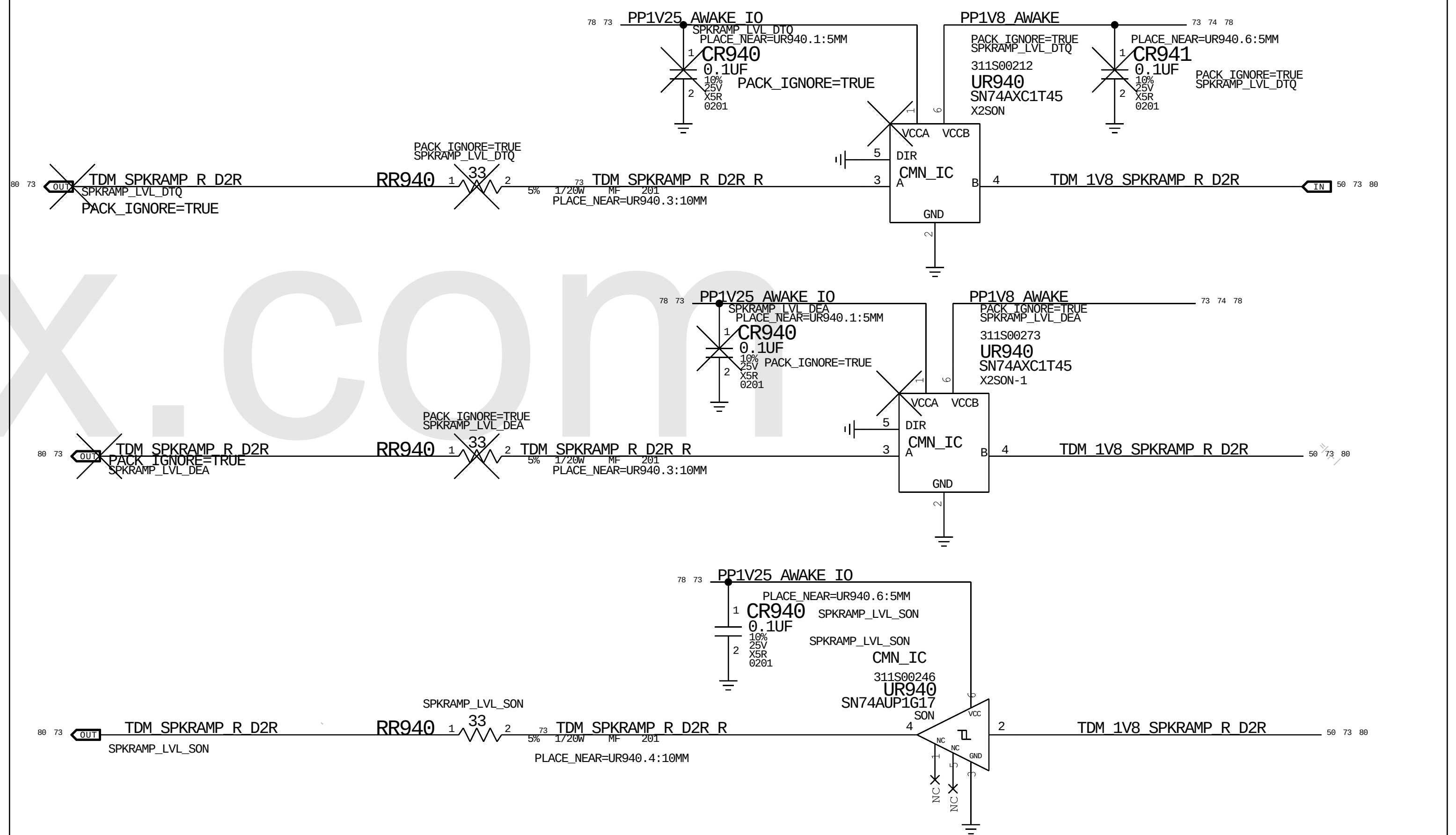
C Right Speaker Amplifier TDM Level Translator



B Left Speaker Amplifier TDM Output Level Translator



D Right Speaker Amplifier TDM Output Level Translator



*** OK2INTEGRATE ***

NOTES:

- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSE/PIN SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
 - SPKRAMP_XX_OUTP/N
 - SPKRAMP_XX_OUTP/N
 - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

AUDIO AMPLIFIERS

BOM_COST_GROUP=AUDIO

*** OK2INTEGRATE ***

NOTES:

- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSE/PIN SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
 - SPKRAMP_XX_OUTP/N
 - SPKRAMP_XX_OUTP/N
 - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

AUDIO AMPLIFIERS

BOM_COST_GROUP=AUDIO

*** OK2INTEGRATE ***

The diagram shows three identical audio amplifier sections, labeled AMP A, AMP B, and AMP C. Each section is centered around a TAS770AC0 DSBGA chip. The chip is connected to a power supply (PP1V8 AWAKE) and ground (GND) through a series of capacitors (CR600-CR603 for AMP A, CR630-CR633 for AMP B, and CR660-CR663 for AMP C). The chip's output pins (A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75, A76, A77, A78, A79, A80, A81, A82, A83, A84, A85, A86, A87, A88, A89, A90, A91, A92, A93, A94, A95, A96, A97, A98, A99, A100) are connected to the speaker through a series of resistors and capacitors. The output of each amplifier is connected to a speaker (SPKRAMP_A, SPCRAMP_B, SPCRAMP_C) through a series of resistors and capacitors. The diagram includes detailed component values and placement notes.

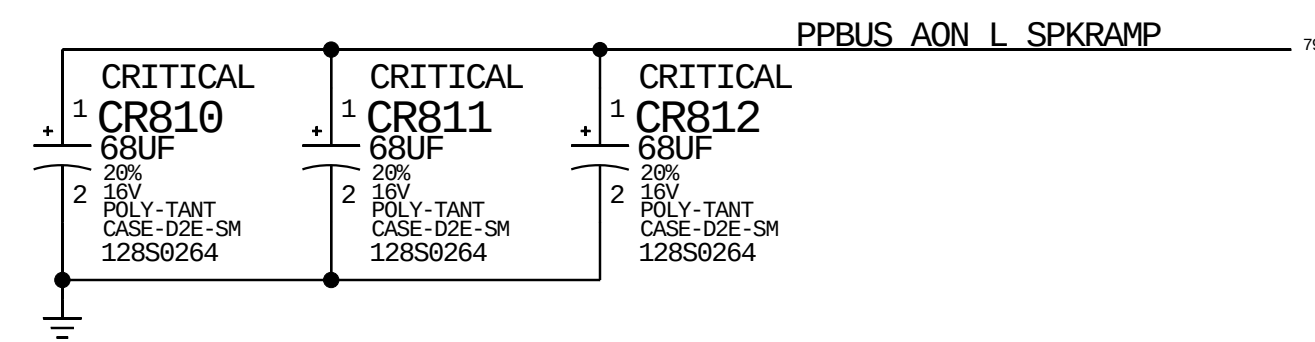
NOTES:

- CHECK THAT SPCRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSE/PIN SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
 - SPCRAMP_XX_OUTP/N
 - SPCRAMP_XX_OUTP/N
 - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

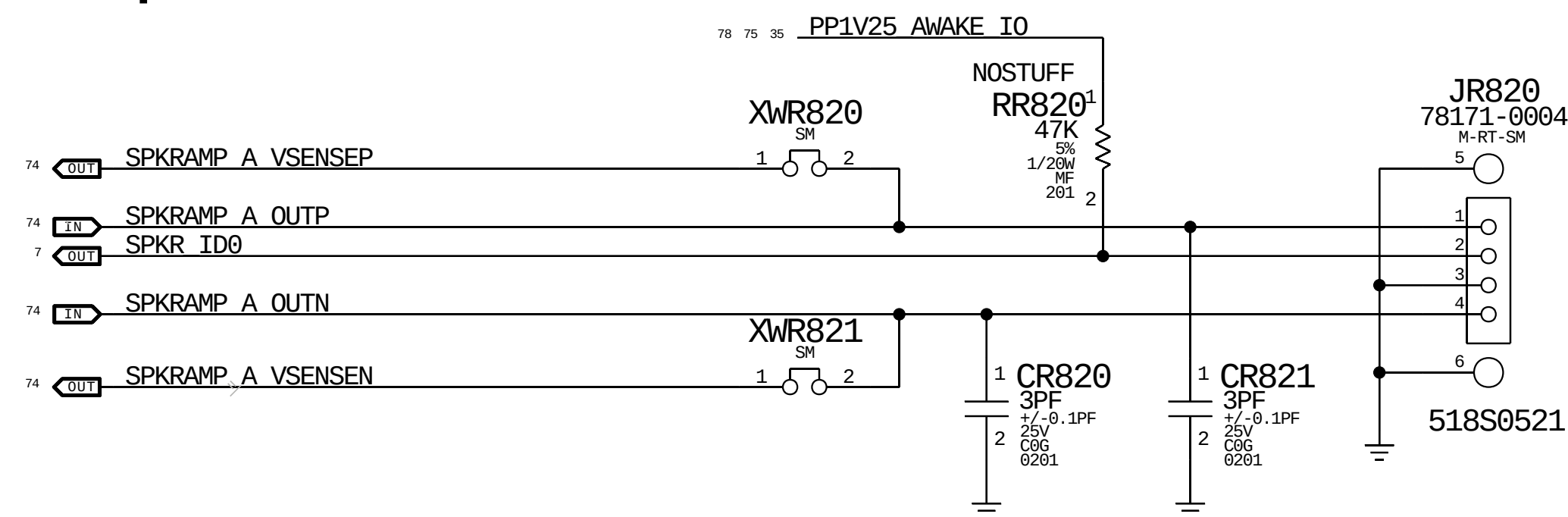
AUDIO AMPLIFIERS

BOM_COST_GROUP=AUDIO

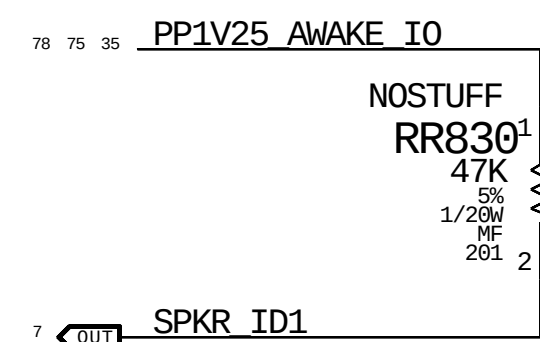
A Left Speaker Amplifier Bulk Capacitors



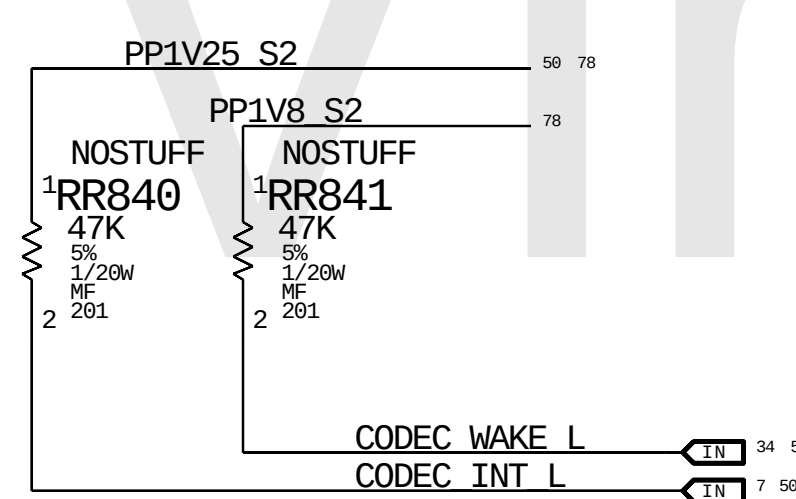
B Left Speaker Connector



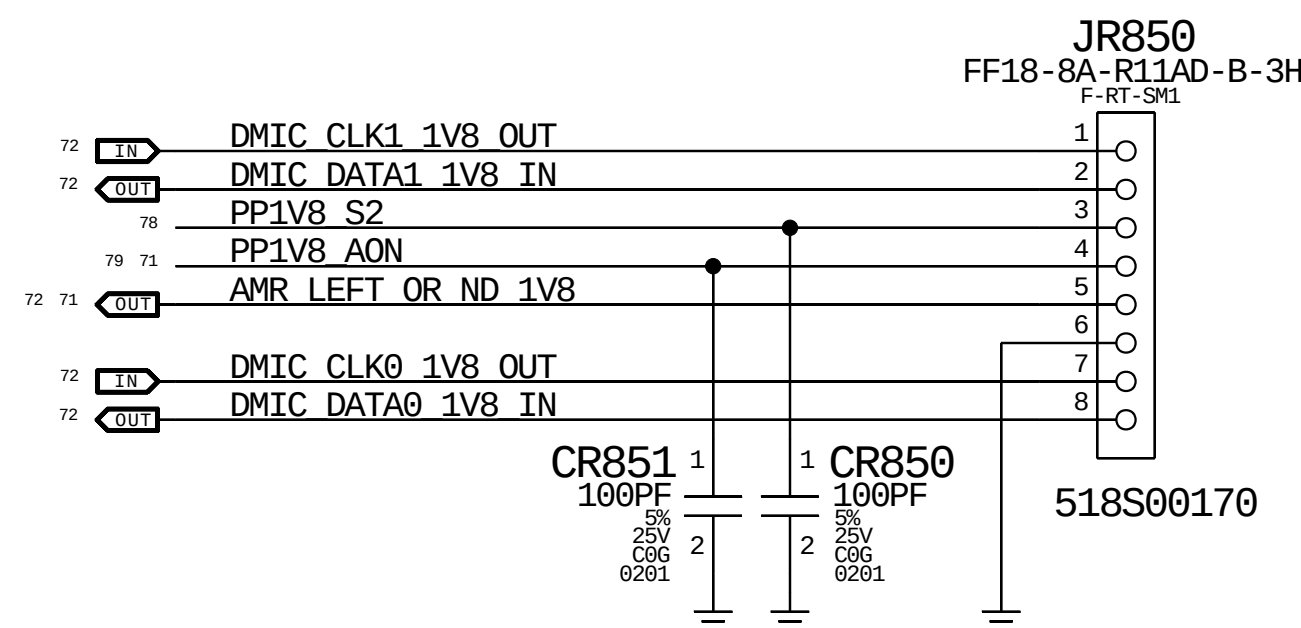
C Right Speaker ID



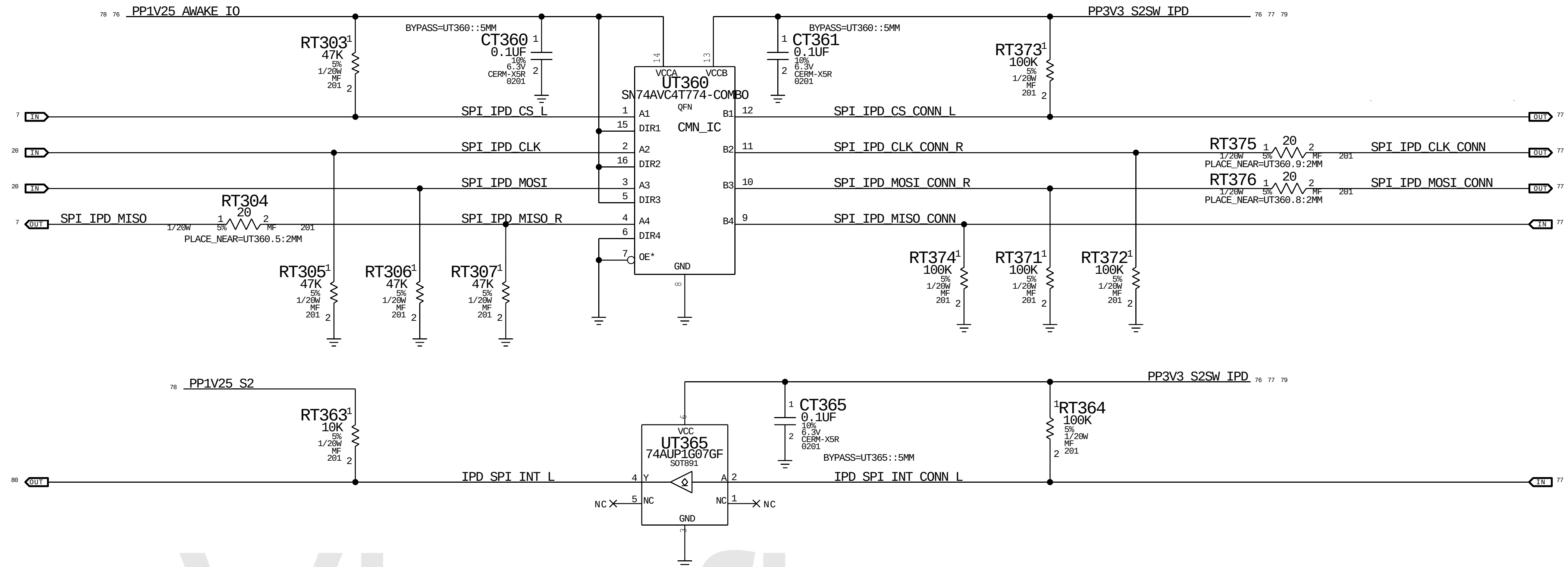
D Audio Jack CODEC Pull-Ups



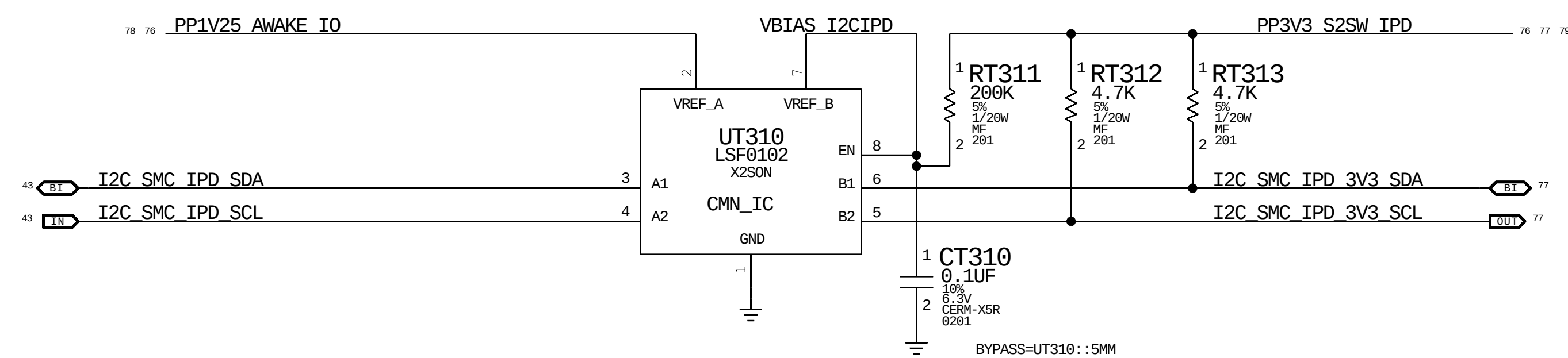
E DMic Connector



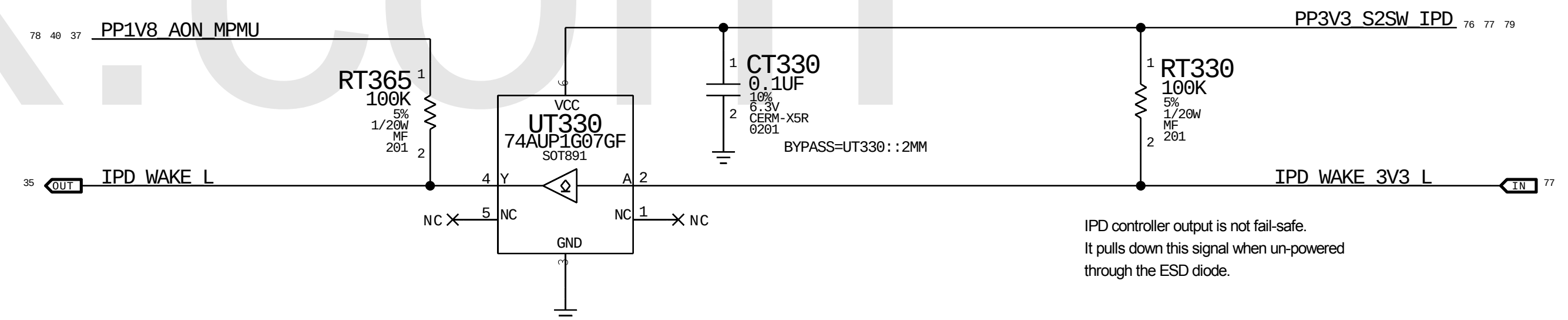
A Trackpad SPI Bus Level Shifter (+1.2V to +3.3V)



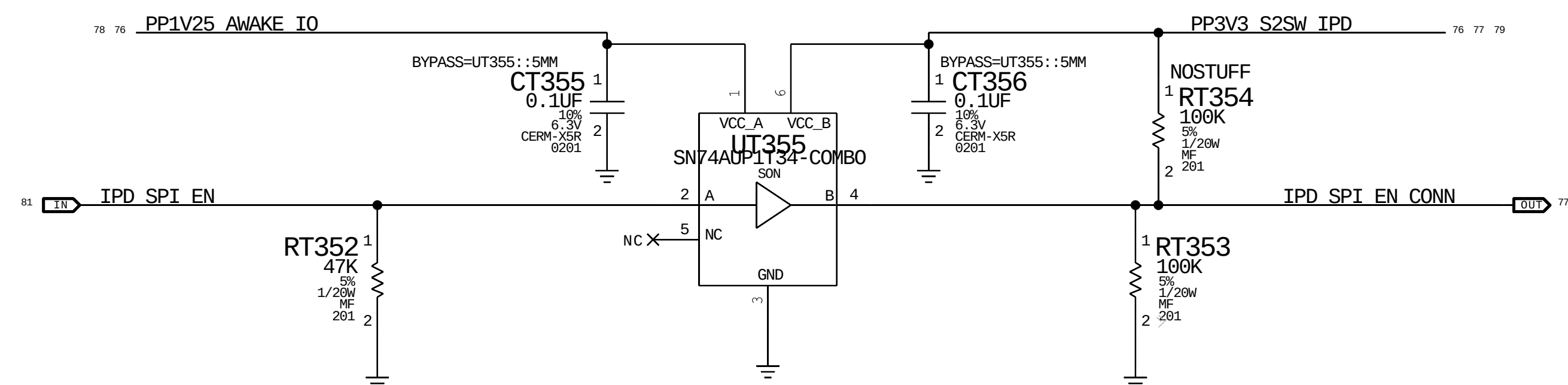
B Trackpad I2C Bus Level Shifter



C Trackpad Wake Level Shifter

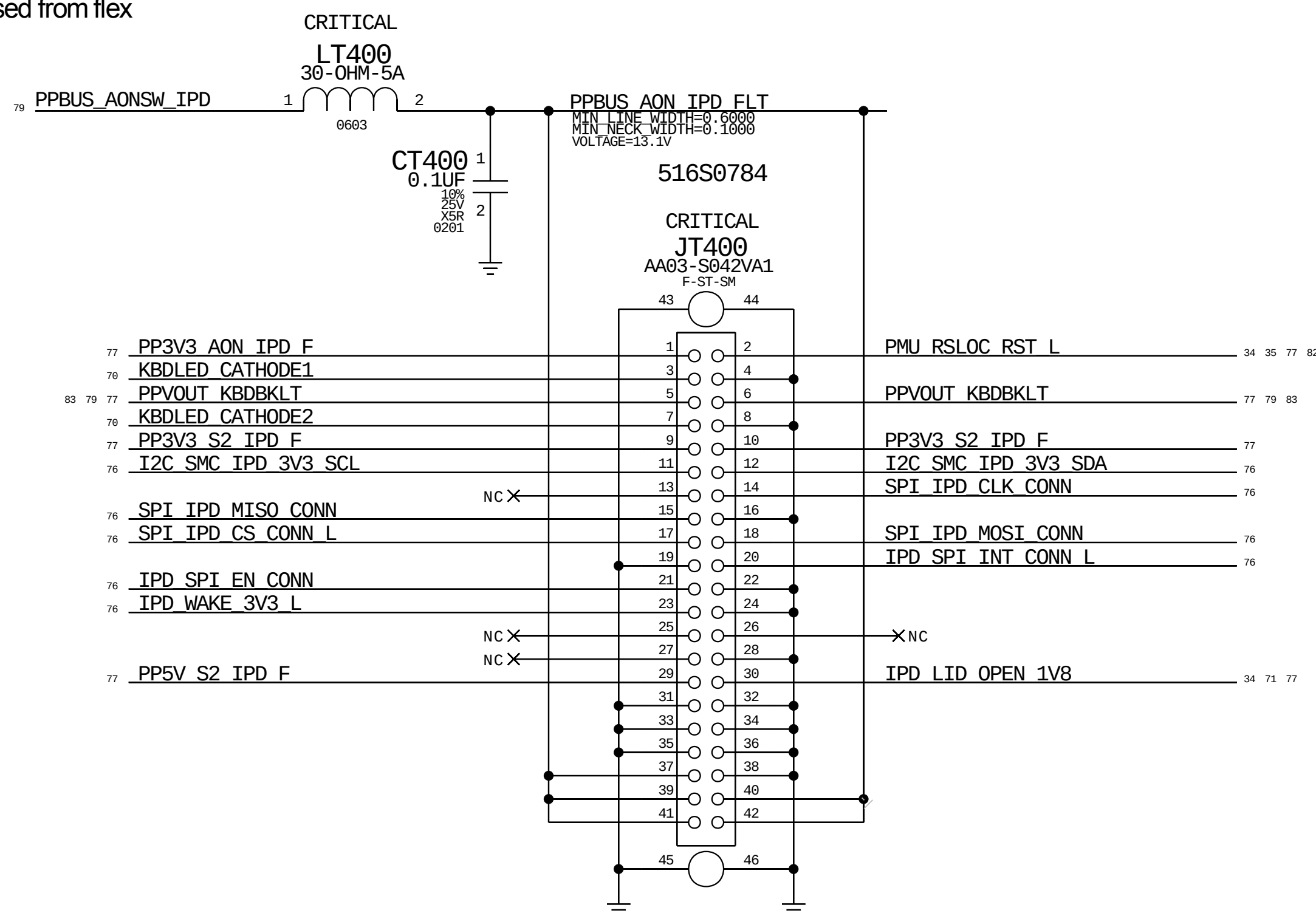


D Trackpad SPI Enable Level Shifter

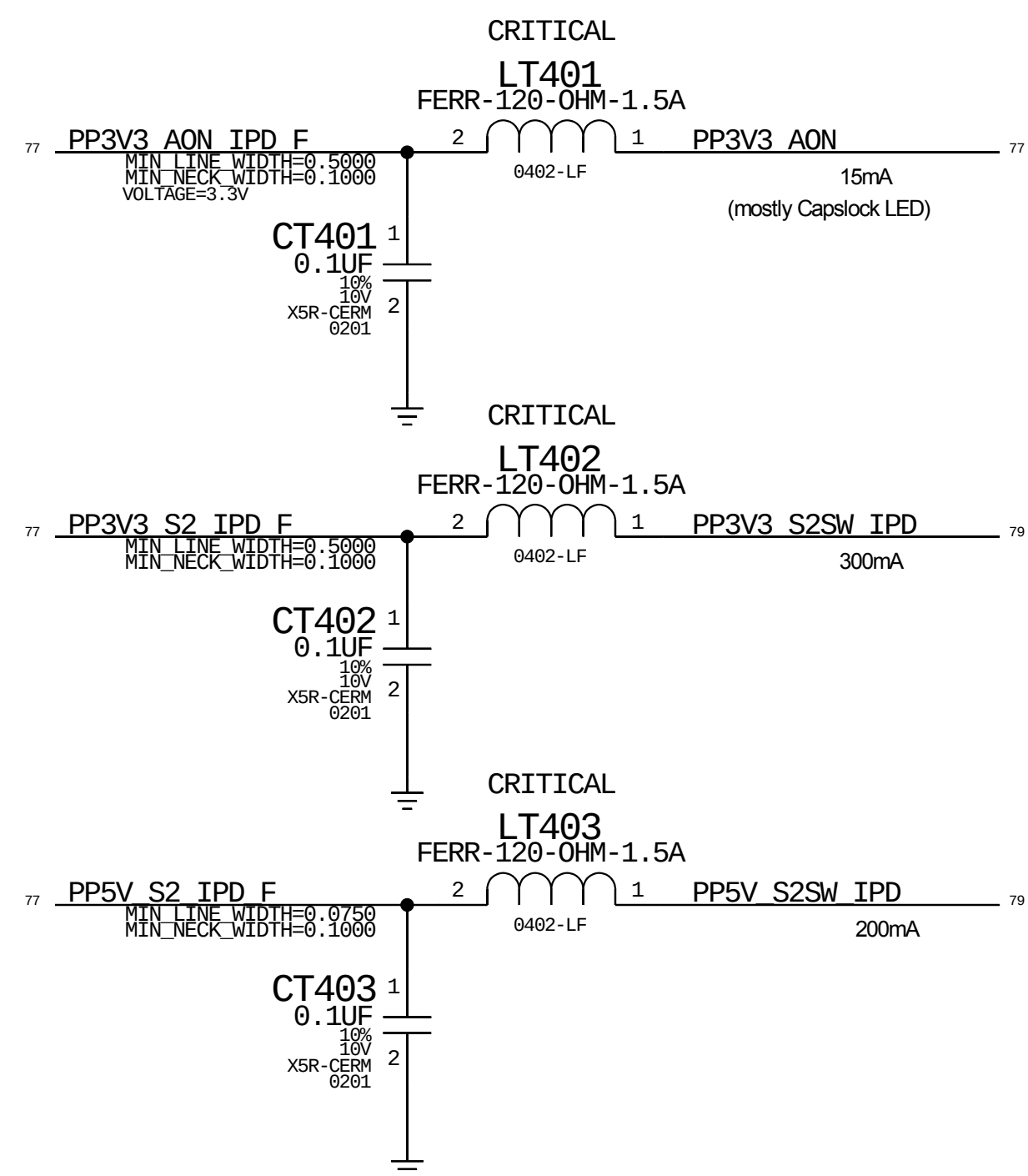


A IPD B2B CONNECTOR

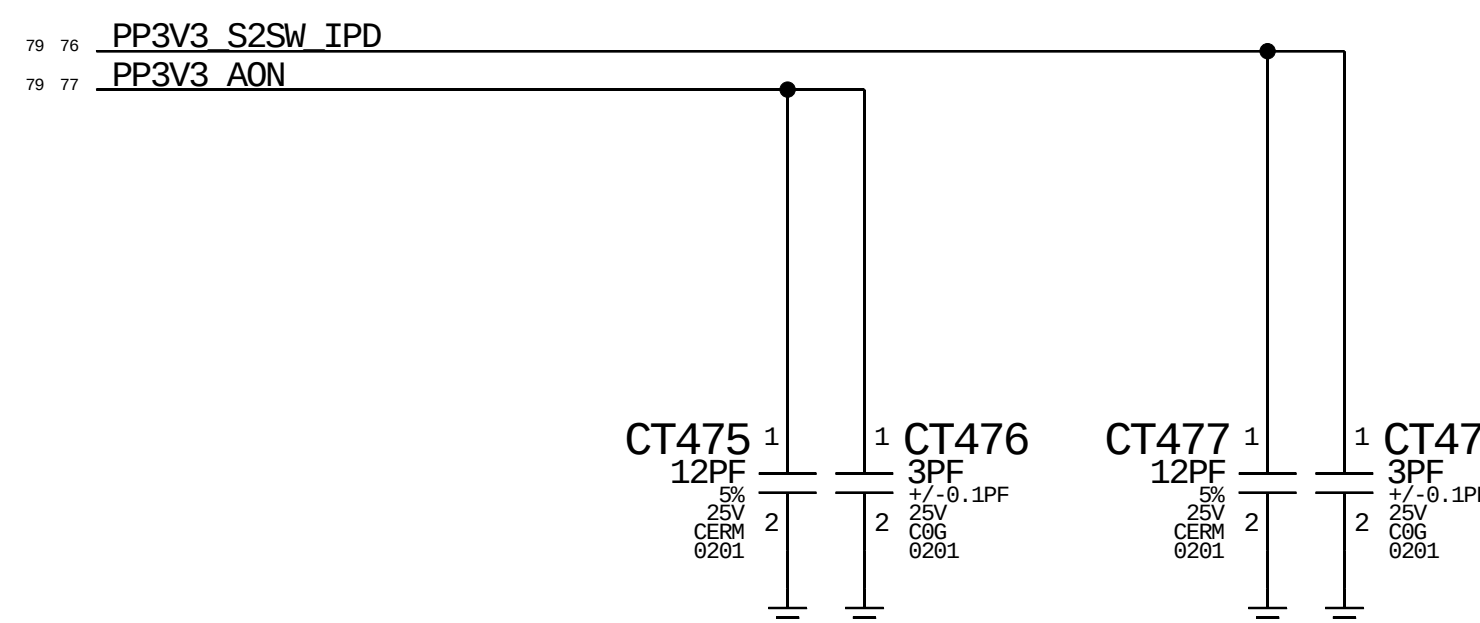
Bottom side contacts used
Pinout reversed from flex



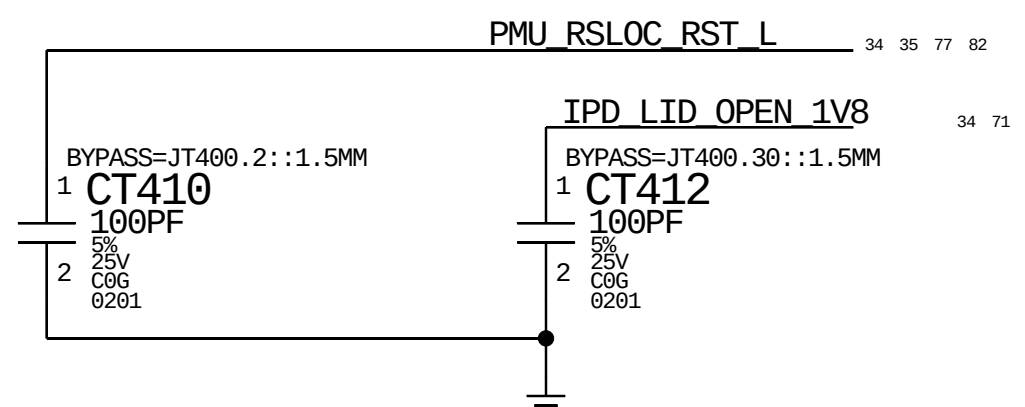
B IPD Power Filters



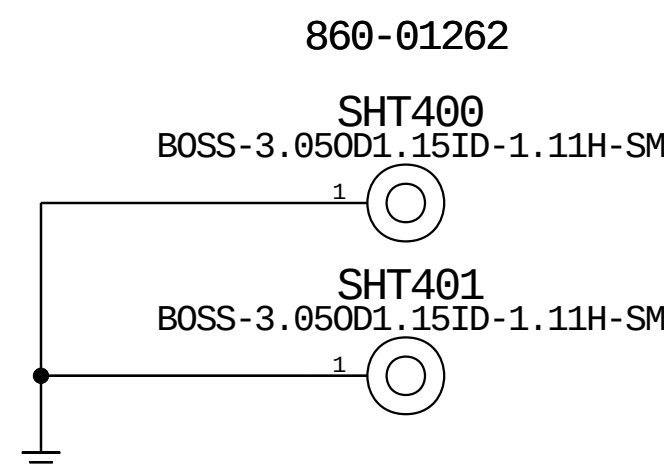
C IPD Desense



D IPD Control

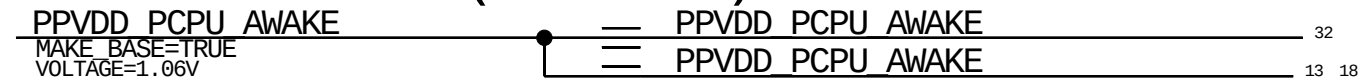


F IPD Connector Bosses

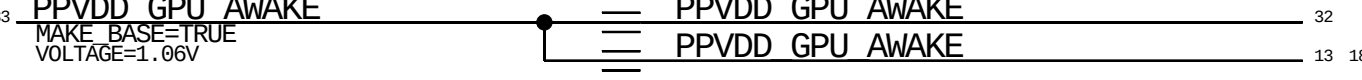


POWER CONNECTIONS

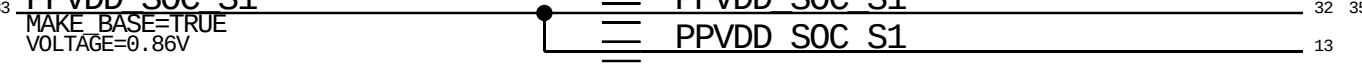
SERA BUCK0 (ACTIVE)



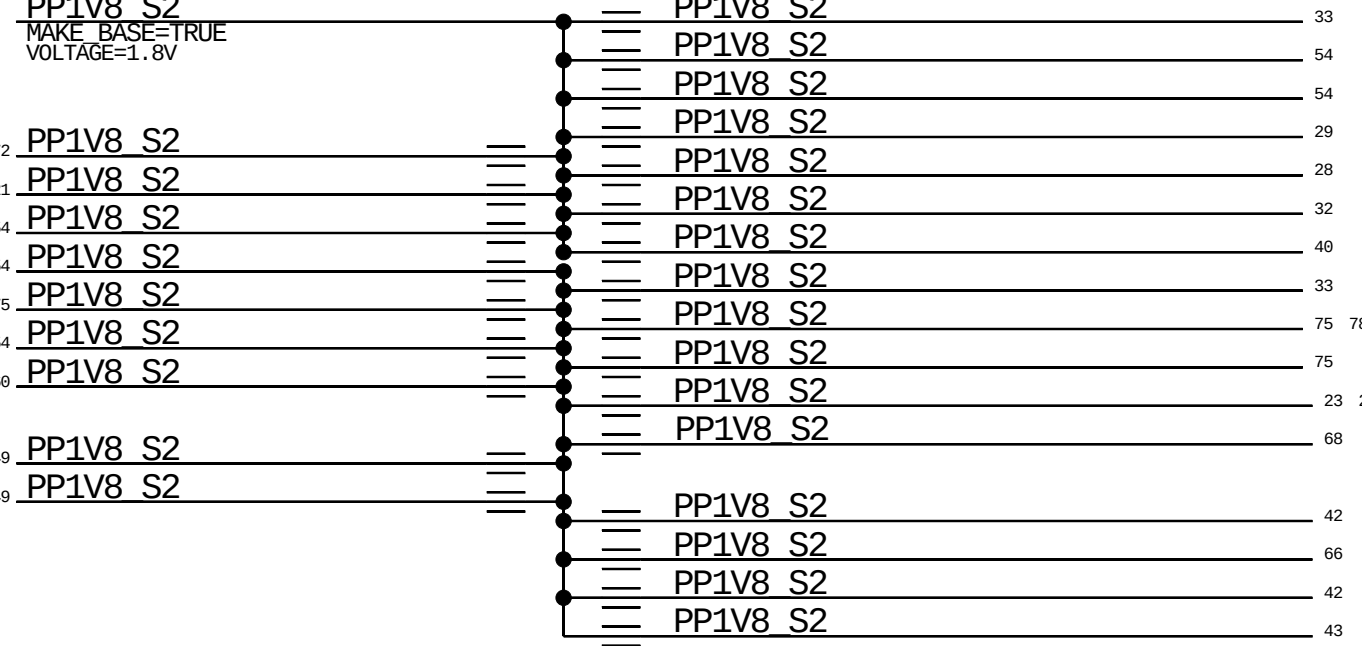
SERA BUCK1 (SW CTRL)



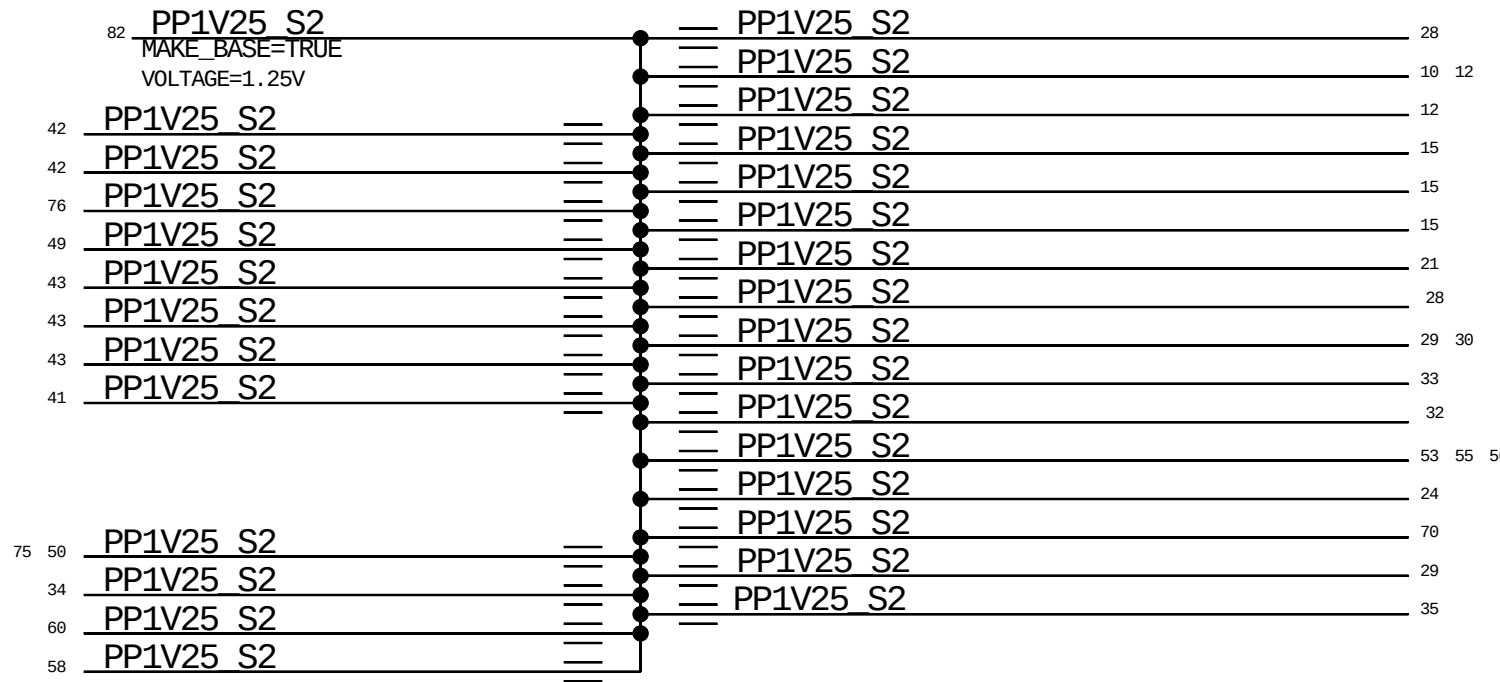
SERA BUCK2 (SLEEP1)



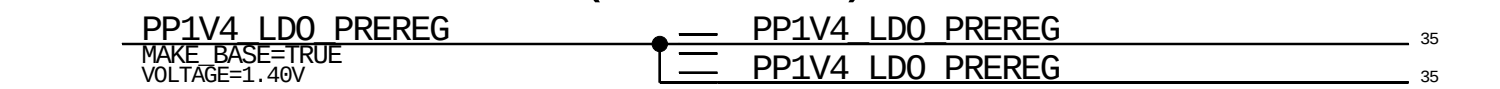
SERA BUCK3 (SLEEP3)



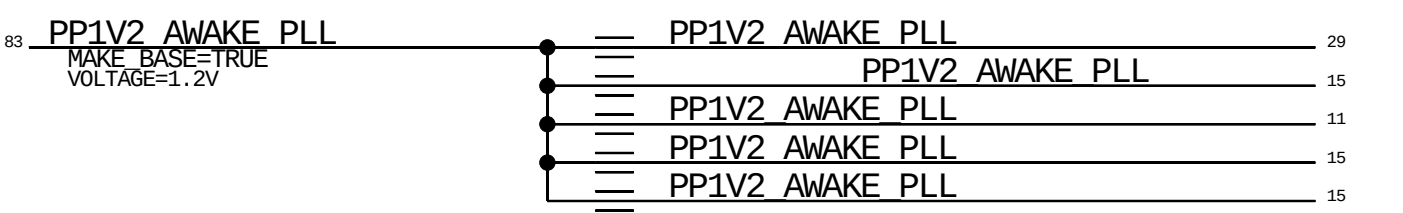
SIMETRA BUCK13 (ACTIVE)



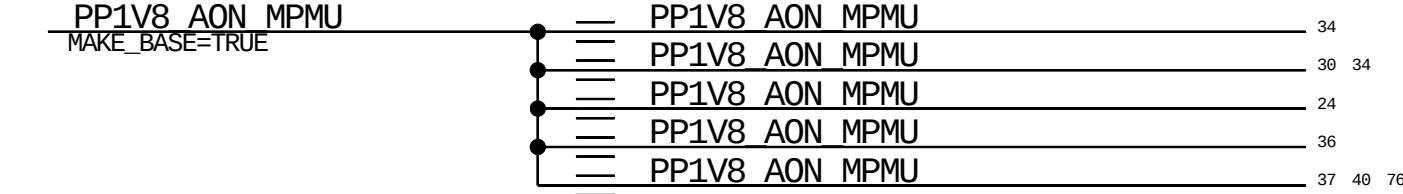
SERA BUCK14 (ACTIVE)



SIMETRA LDO8 (SLEEP2)

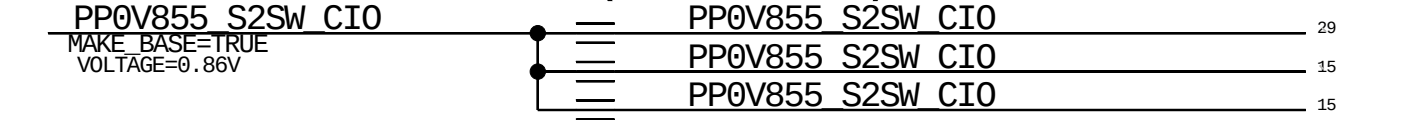


SERA LDO9 (ACTIVE)

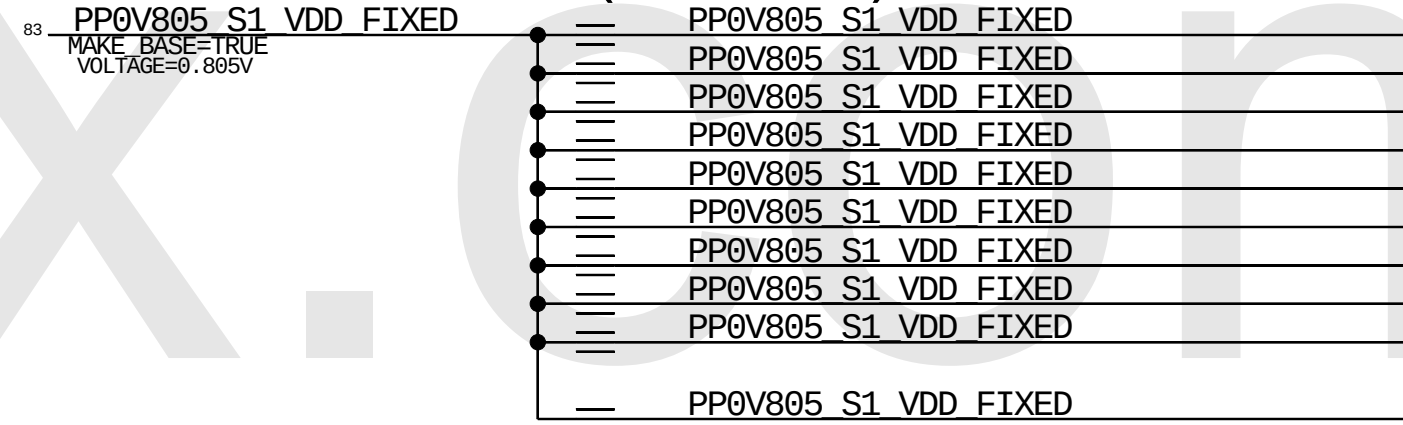


SERA LDO10 (ACTIVE)

SIMETRA LDO11 (SLEEP2)



SIMETRA LDO12 (SLEEP2)

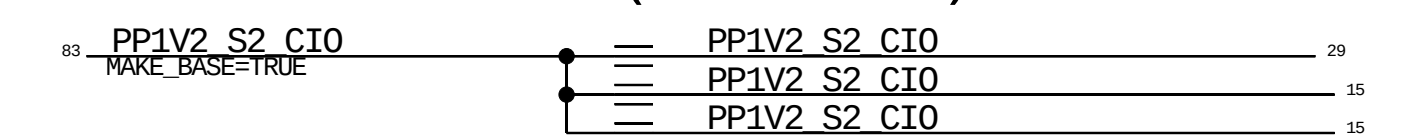


SERA LDO13 (SW CTRL)

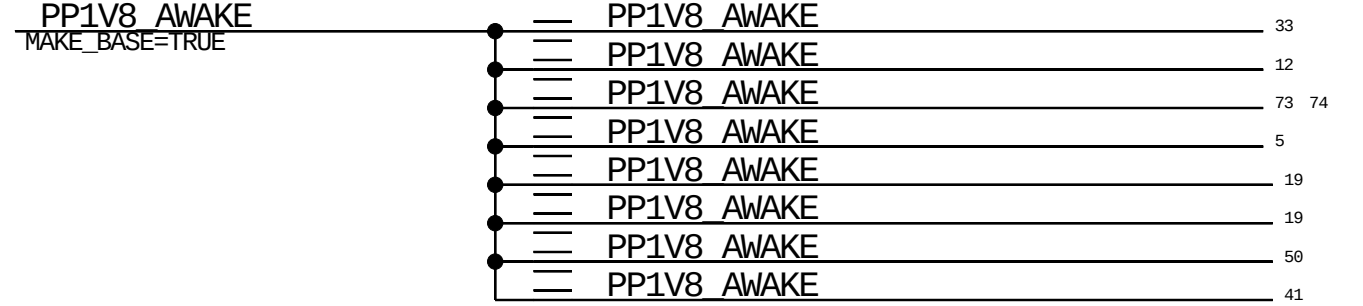
SERA LDO16 (SW CTRL)

SERA LDO19 (SPARE)

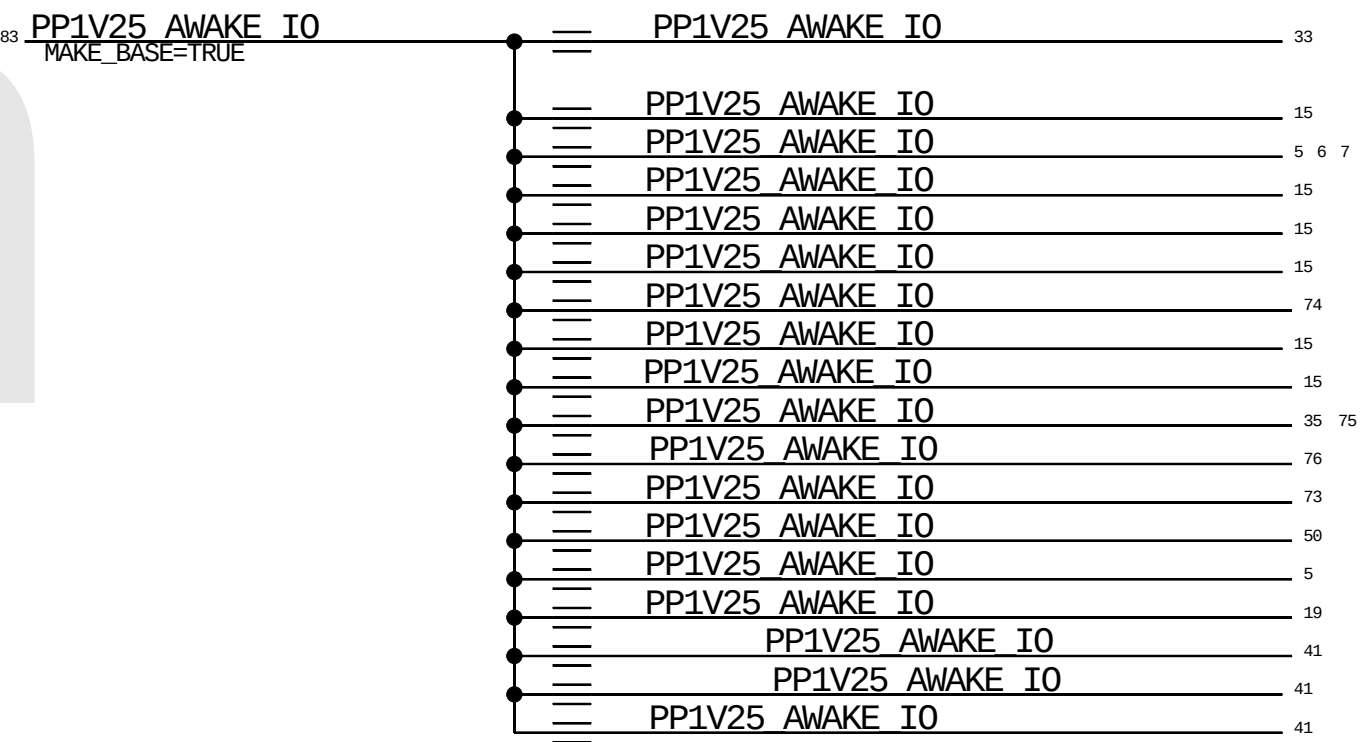
SIMETRA LDO20 (SW CTRL)



SERA SW1 (ACTIVE)

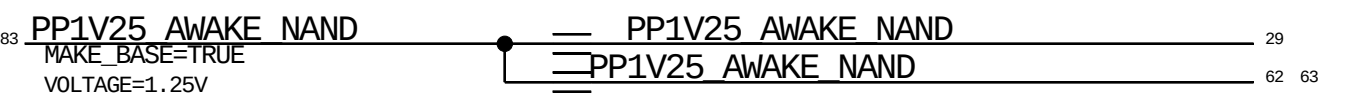


SERA SW3 (ACTIVE)

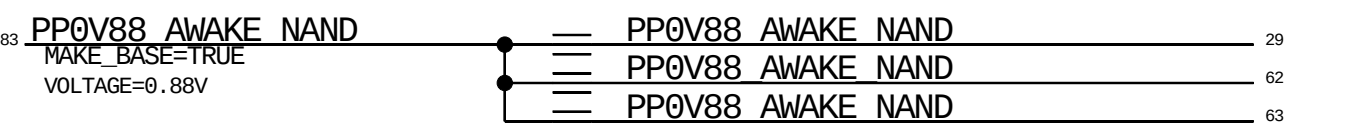


SIMETRA SW4 (SLEEP2)

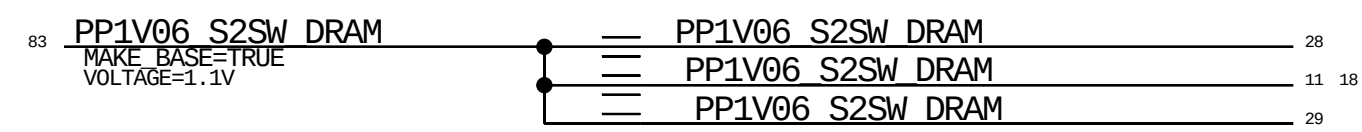
SIMETRA SW5 (SLEEP2)



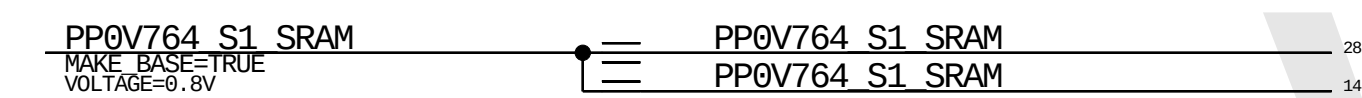
SIMETRA SW6 (SLEEP2) PARALLEL SIMETRA SW7 (SLEEP2) PARALLEL



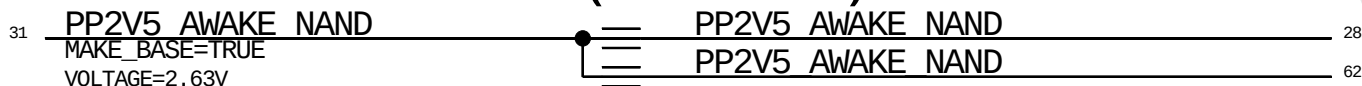
SIMETRA BUCK4 (SLEEP3)



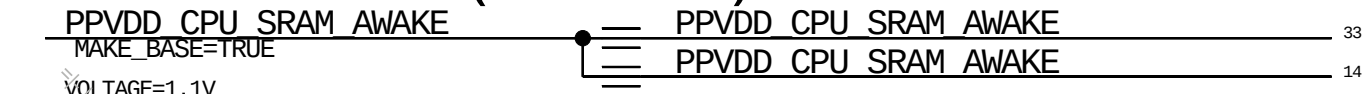
SIMETRA BUCK5 (SLEEP1)



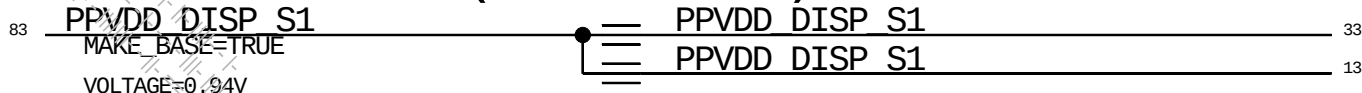
SIMETRA BUCK6 (ACTIVE)



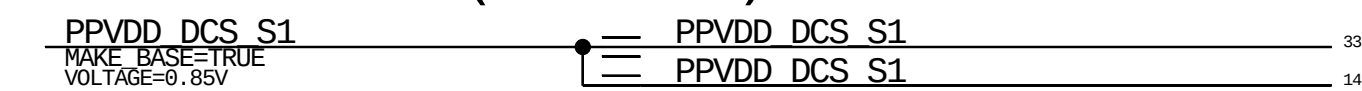
SERA BUCK7 (ACTIVE)



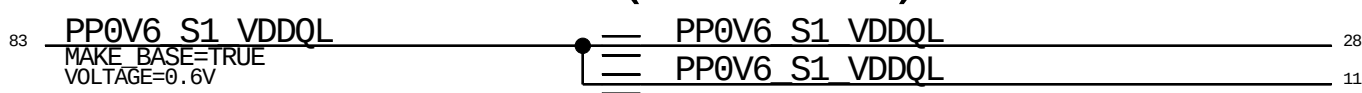
SERA BUCK8 (SW CTRL)



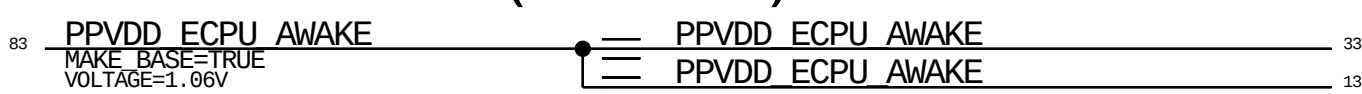
SERA BUCK9 (SLEEP1)



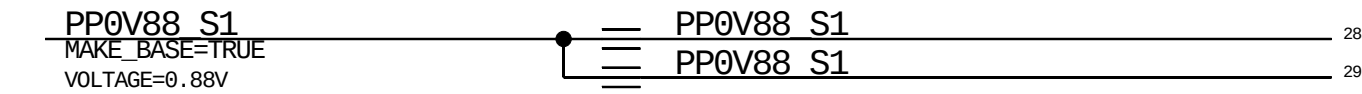
SIMETRA BUCK10 (SLEEP1)



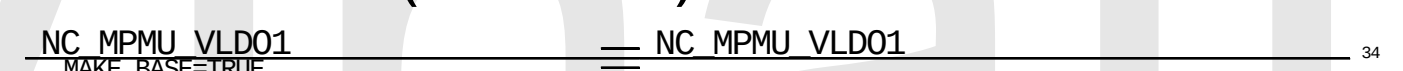
SERA BUCK11 (ACTIVE)



SIMETRA BUCK12 (ACTIVE)

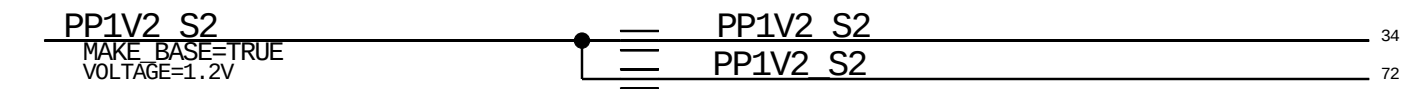


SERA LDO1 (SLEEP2)

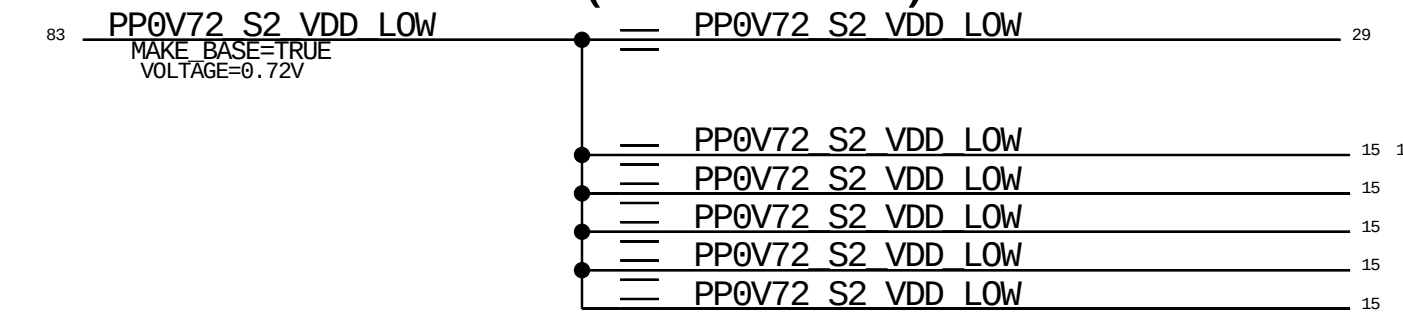


SERA LDO2 (SLEEP2)

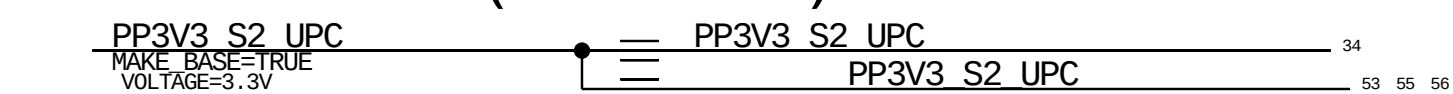
SERA LDO3 (SLP_S2R)



SIMETRA LDO4 (SW CTRL)



SERA LDO7 (SW CTRL)



U7550 - 5V G3S

Legend:

- PPBUS AON: Power Plane AON
- PPBUS 5VS2 VIN: Power Plane 5VS2 VIN
- PPBUS 3V3S2 VIN: Power Plane 3V3S2 VIN
- PPBUS AON L SPKRAMP: Power Plane AON L SPKRAMP
- PPBUS AONSW IPD: Power Plane AONSW IPD
- PPDCIN AONSW: Power Plane PPDCIN AONSW
- PP5V S2: Power Plane 5V S2
- PP5V S2 KBDLED: Power Plane 5V S2 KBDLED
- PP5V AON P3V8VRLDO: Power Plane 5V AON P3V8VRLDO
- PP5V SW LCD: Power Plane 5V SW LCD
- PP5V S2SW IPD: Power Plane 5V S2SW IPD

Diagram Details:

- PPBUS AON:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 83.
- PPBUS 5VS2 VIN:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 44.
- PPBUS 3V3S2 VIN:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 44.
- PPBUS AON L SPKRAMP:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 46.
- PPBUS AONSW IPD:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 48.
- PPDCIN AONSW:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=1.3-1V, MAKE BASE=TRUE. Connected to 53.
- PP5V S2:** MIN LINE WIDTH=0.2000, MIN NECK WIDTH=0.1000, VOLTAGE=5V, MAKE BASE=TRUE. Connected to 38. Sourced from PBUS. Enabled by P5V_G3S_EN.
- PP5V S2 KBDLED:** MIN LINE WIDTH=0.0970, MIN NECK WIDTH=0.1000, VOLTAGE=5V, MAKE BASE=TRUE. Connected to 46.
- PP5V AON P3V8VRLDO:** MIN LINE WIDTH=0.2000, MIN NECK WIDTH=0.1000, VOLTAGE=3.3V, MAKE BASE=TRUE. Connected to 25.
- PP5V SW LCD:** MIN LINE WIDTH=0.2000, MIN NECK WIDTH=0.1000, VOLTAGE=5V, MAKE BASE=TRUE. Connected to 68.
- PP5V S2SW IPD:** MIN LINE WIDTH=0.2000, MIN NECK WIDTH=0.1000, VOLTAGE=5V, MAKE BASE=TRUE. Connected to 40.

PP3V3 S2

Sourced from PBus
Enabled by ????

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2

PP3V3 S2 WLBT

PP3V3 S2 WLBT

MIN LINE WIDTH=0.1000
MIN NECK WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3 S2 WLBT

PP3V3 S2SW SNS

PP3V3 S2SW SNS

MIN LINE WIDTH=0.0978
MIN NECK WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3 S2SW SNS

PP3V3 S2SW IPD

PP3V3 S2SW IPD

MIN LINE WIDTH=0.0978
MIN NECK WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3 S2SW IPD

PP3V3 SW LCD

PP3V3 SW LCD

MIN LINE WIDTH=0.2000
MIN NECK WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3 SW LCD

PP3V3 A0N

Sourced from PBus

PP3V3 A0N

PP3V3 A0N

PP3V3 A0N

PP3V3 A0N

PP1V8 A0N

MAKE_BASE=TRUE
VOLTAGE=1.8V

PP1V8 A0N

PP1V8 A0N

PP1V8 A0N

PP1V8 A0N

PP1V8 S2SW VDD1

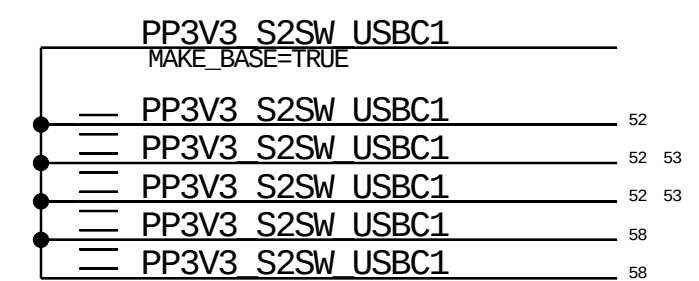
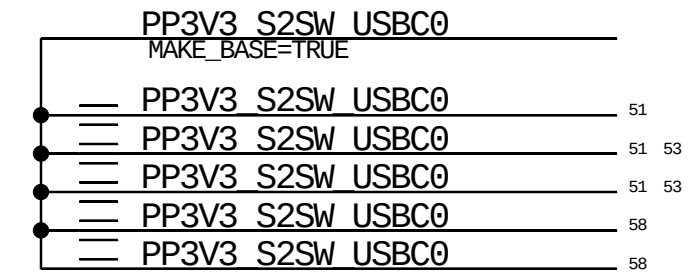
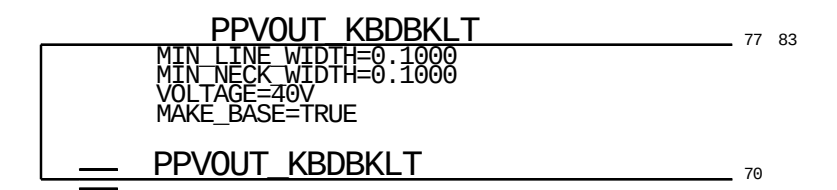
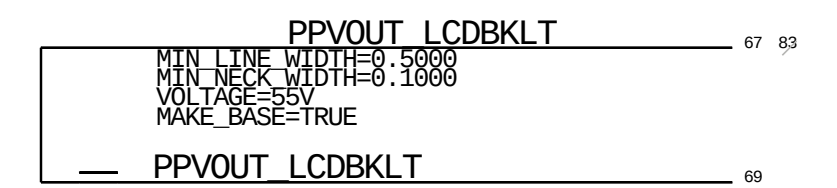
MAKE_BASE=TRUE
VOLTAGE=1.8V

PP1V8 S2SW VDD1

PP1V8 S2SW VDD1

Timing diagram for PP3V8_AON_VDDMAIN. The signal is high for most of the time, with a brief low pulse. The signal is labeled 'MAKE BASE=TRUE' and 'VOLTAGE=3.3V'. The signal is connected to multiple pins, with pin numbers 26, 32, 34, 35, 28, 29, 50, 40, 36, 36, 27, 21, 51, 52, 22, 32, and 37 listed on the right. The signal is also connected to a ground symbol.

GND
VOLTAGE=0V
MIN LINE WIDTH=0.1000
MIN NECK WIDTH=0.0800



7	NC_DFR_1V8_DISP_INT	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_INT
7	NC_DFR_1V8_DISP_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_RESET_L
7	NC_DFR_1V8_TOUCH_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_TOUCH_RESET_L
8	NC_DFR_DISP_TE	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_DISP_TE
7	NC_DFR_PWR_EN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_PWR_EN
7	NC_HDMI_CEC_AOP_RX	==	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_RX
10	NC_HDMI_CEC_AOP_TX	==	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_TX
10	NC_HDMI_HPD_AOP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_HPD_AOP
8	NC_MIP1_DFR_CLKN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_DFR_CLKN
8	NC_MIP1_DFR_CLKP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_DFR_CLKP
8	NC_MIP1_DFR_DATAN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_DFR_DATAN
8	NC_MIP1_DFR_DATAP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_DFR_DATAP
9	NC_PCIE_CLK100M_ENETN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETN
9	NC_PCIE_CLK100M_ENETP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETP
9	NC_PCIE_CLK100M_USBHCN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCN
9	NC_PCIE_CLK100M_USBHCP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCP
9	NC_PCIE_ENET_D2RN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RN
9	NC_PCIE_ENET_D2RP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RP
9	NC_PCIE_ENET_R2DCN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCN
9	NC_PCIE_ENET_R2DCP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCP
9	NC_PCIE_USBHC_D2RN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RN
9	NC_PCIE_USBHC_D2RP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RP
9	NC_PCIE_USBHC_R2DCN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCN
9	NC_PCIE_USBHC_R2DCP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCP
9	NC_SMC_FAN_PWM_SMC_STL_LED_PWM	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_PWM_SMC_STL_LED_PWM
10	NC_SMC_FAN_TACH	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_TACH

8	NC_SPI_DISP_BKLT_MOSTI	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MOSTI
8	NC_SPI_DISP_BKLT_MISO	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MISO
10	NC_SPI_DP2HDMI_HOLD_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DP2HDMI_HOLD_L
10	NC_NUB_SWD_TMS1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_NUB_SWD_TMS1
21	NC_I2C_SE_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SCL
21	NC_I2C_SE_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SDA

7	NC_DFR_TOUCH_INT_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_INT_L
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7	NC_UART_TCON_R2D	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_TCON_R2D
7	NC_ADCD_BURST_EN_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ADCD_BURST_EN_L
10	NC_ADCD_ID	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ADCD_ID
10	NC_CCG_SMC_I2C_INT_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_CCG_SMC_I2C_INT_L
8	NC_BKLT_FAULT_INT_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_FAULT_INT_L
8	NC_DISP_BKLT_LSYNC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_BKLT_LSYNC
9	NC_ENET_CLKREQ_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_CLKREQ_L
9	NC_ENET_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_RESET_L
9	NC_USBHC_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_USBHC_RESET_L
10	NC_DFR_TOUCH_CLK32K_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_CLK32K_RESET_L
10	NC_AOP_FUNC0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC0
10	NC_AOP_FUNC3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC3
10	NC_AOP_FUNC2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC2
10	NC_SPI_R1_CS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_R1_CS_L
10	NC_BKLT_PWR_ON	==	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_PWR_ON
61	NC_RE_BT_DED	==	MAKE_BASE=TRUE	NO_TEST=1	NC_RE_BT_DED
8	NC_MIP1_FTCAM_DATA1P	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_FTCAM_DATA1P
8	NC_MIP1_FTCAM_DATA1N	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIP1_FTCAM_DATA1N

72	NC_DMIC_CLK2_1V8_OUT_R_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_1V8_OUT_R_IC
72	NC_DMIC_CLK2_IN_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_IN_IC
72	NC_DMIC_DATA2_1V8_IN_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_1V8_IN_IC
72	NC_DMIC_DATA2_SEC_OUT_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_SEC_OUT_IC
72	NC_FTCAM_ENABLE_SEC_1V8_OUT_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_SEC_1V8_OUT_IC
72	NC_IRCAM_ENABLE_IN_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_IN_IC
72	NC_IRCAM_ENABLE_SEC_1V8_OUT_IC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_SEC_1V8_OUT_IC
72	FTCAM_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	FTCAM_RESET_L
72	NC_SEP_IRCAM_DISABLE_IC_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SEP_IRCAM_DISABLE_IC_L
72	NC_FTCAM_ENABLE_IN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_IN

7	NC_ENET_SYNC_1588	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_SYNC_1588
7	NC_SPI_DFR_CS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DFR_CS_L
7	NC_SWD_UPC_SWDIO1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_UPC_SWDIO1
10	NC_ALS_INT_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ALS_INT_L
7	NC_SOC_TRIGGER2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_TRIGGER2

60	NC_BT_GPIO_4	==	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_GPIO_4
60	NC_SPMI_WLBT_CLK_1V8	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_CLK_1V8
60	NC_SPMI_WLBT_DAT_1V8	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_DAT_1V8

7	TOUCHID_PWR_EN	==	MAKE_BASE=TRUE		TOUCHID_PWR_EN
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50	USB2_ATC0_LS_P	==	MAKE_BASE=TRUE	USB2_ATC0_LS_P	50
50	USB2_ATC0_LS_N	==	MAKE_BASE=TRUE	USB2_ATC0_LS_N	50
50	USB2_ATC1_LS_P	==	MAKE_BASE=TRUE	USB2_ATC1_LS_P	50
50	USB2_ATC1_LS_N	==	MAKE_BASE=TRUE	USB2_ATC1_LS_N	50
50	USB_DBG_LS_P	==	MAKE_BASE=TRUE	USB_DBG_LS_P	54
50	USB_DBG_LS_N	==	MAKE_BASE=TRUE	USB_DBG_LS_N	54

30	CHGR_INT_L	==	MAKE_BASE=TRUE	CHGR_INT_L	24
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51	USBC_ATC0_R2D_P<1>	==	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<1>	51
51	USBC_ATC0_R2D_N<1>	==	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<1>	51
51	USBC0_D2R_P<1>	==	MAKE_BASE=TRUE	USBC0_D2R_P<1>	57
51	USBC0_D2R_N<1>	==	MAKE_BASE=TRUE	USBC0_D2R_N<1>	57
51	USBC_ATC0_R2D_P<2>	==	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<2>	51
51	USBC_ATC0_R2D_N<2>	==	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<2>	51
51	USBC0_D2R_P<2>	==	MAKE_BASE=TRUE	USBC0_D2R_P<2>	57
51	USBC0_D2R_N<2>	==	MAKE_BASE=TRUE	USBC0_D2R_N<2>	57
51	USBC_ATC0_D2R_C_P<1>	==	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<1>	51
51	USBC_ATC0_D2R_C_N<1>	==	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<1>	51
51	USBC0_R2D_CR_P<1>	==	MAKE_BASE=TRUE	USBC0_R2D_CR_P<1>	57
51	USBC0_R2D_CR_N<1>	==	MAKE_BASE=TRUE	USBC0_R2D_CR_N<1>	57
51	USBC_ATC0_D2R_C_P<2>	==	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<2>	51
51	USBC_ATC0_D2R_C_N<2>	==	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<2>	51
51	USBC0_R2D_CR_P<2>	==	MAKE_BASE=TRUE	USBC0_R2D_CR_P<2>	57
51	USBC0_R2D_CR_N<2>	==	MAKE_BASE=TRUE	USBC0_R2D_CR_N<2>	57

52	USBC_ATC1_R2D_P<1>	==	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<1>	52
52	USBC_ATC1_R2D_N<1>	==	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<1>	52
52	USBC1_D2R_P<1>	==	MAKE_BASE=TRUE	USBC1_D2R_P<1>	57
52	USBC1_D2R_N<1>	==	MAKE_BASE=TRUE	USBC1_D2R_N<1>	57
52	USBC_ATC1_R2D_P<2>	==	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<2>	52
52	USBC_ATC1_R2D_N<2>	==	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<2>	52
52	USBC1_D2R_P<2>	==	MAKE_BASE=TRUE	USBC1_D2R_P<2>	57
52	USBC1_D2R_N<2>	==	MAKE_BASE=TRUE	USBC1_D2R_N<2>	57
52	USBC_ATC1_D2R_C_P<1>	==	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<1>	52
52	USBC_ATC1_D2R_C_N<1>	==	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<1>	52
52	USBC1_R2D_CR_P<1>	==	MAKE_BASE=TRUE	USBC1_R2D_CR_P<1>	57
52	USBC1_R2D_CR_N<1>	==	MAKE_BASE=TRUE	USBC1_R2D_CR_N<1>	57
52	USBC_ATC1_D2R_C_P<2>	==	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<2>	52
52	USBC_ATC1_D2R_C_N<2>	==	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<2>	52
52	USBC1_R2D_CR_P<2>	==	MAKE_BASE=TRUE	USBC1_R2D_CR_P<2>	57
52	USBC1_R2D_CR_N<2>	==	MAKE_BASE=TRUE	USBC1_R2D_CR_N<2>	57

7	UART_TCON_D2R	==	MAKE_BASE=TRUE	UART_TCON_D2R	67
30	IPD_SPI_INT_L	==	MAKE_BASE=TRUE	IPD_SPI_INT_L	76

54	SOC_DOCK_CONNECT	==	MAKE_BASE=TRUE	SOC_DOCK_CONNECT	10
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73	SPKRAMP_RESET_L	==	MAKE_BASE=TRUE	SPKRAMP_RESET_L	7
73	TDM_SPKRAMP_L_BCLK	==	MAKE_BASE=TRUE	TDM_SPKRAMP_L_BCLK	20
73	TDM_SPKRAMP_L_FSYNC	==	MAKE_BASE=TRUE	TDM_SPKRAMP_L_FSYNC	20
73	TDM_SPKRAMP_L_R2D	==	MAKE_BASE=TRUE	TDM_SPKRAMP_L_R2D	20
73	TDM_SPKRAMP_L_D2R	==	MAKE_BASE=TRUE	TDM_SPKRAMP_L_D2R	7
74	TDM_1V8_SPKRAMP_L_BCLK	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_BCLK	73
74	TDM_1V8_SPKRAMP_L_FSYNC	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_FSYNC	73
74	TDM_1V8_SPKRAMP_L_R2D	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_R2D	73
74	TDM_1V8_SPKRAMP_L_D2R	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_D2R	73
73	TDM_SPKRAMP_R_BCLK	==	MAKE_BASE=TRUE	TDM_SPKRAMP_R_BCLK	20
73	TDM_SPKRAMP_R_FSYNC	==	MAKE_BASE=TRUE	TDM_SPKRAMP_R_FSYNC	20
73	TDM_SPKRAMP_R_R2D	==	MAKE_BASE=TRUE	TDM_SPKRAMP_R_R2D	20
73	TDM_SPKRAMP_R_D2R	==	MAKE_BASE=TRUE	TDM_SPKRAMP_R_D2R	7
73	TDM_1V8_SPKRAMP_R_BCLK	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_BCLK	50
73	TDM_1V8_SPKRAMP_R_FSYNC	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_FSYNC	50
73	TDM_1V8_SPKRAMP_R_R2D	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_R2D	50
73	TDM_1V8_SPKRAMP_R_D2R	==	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_D2R	50

60	TPT_WLAN_JTAG_TCK	==	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TCK	
60	TPT_WLAN_JTAG_TMS	==	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TMS	
60	TPT_WLAN_JTAG_TRSTN	==	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TRSTN	
61	TPT_WLAN_JTAG_TDI	==	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDI	
61	TPT_WLAN_JTAG_TDO	==	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDO	

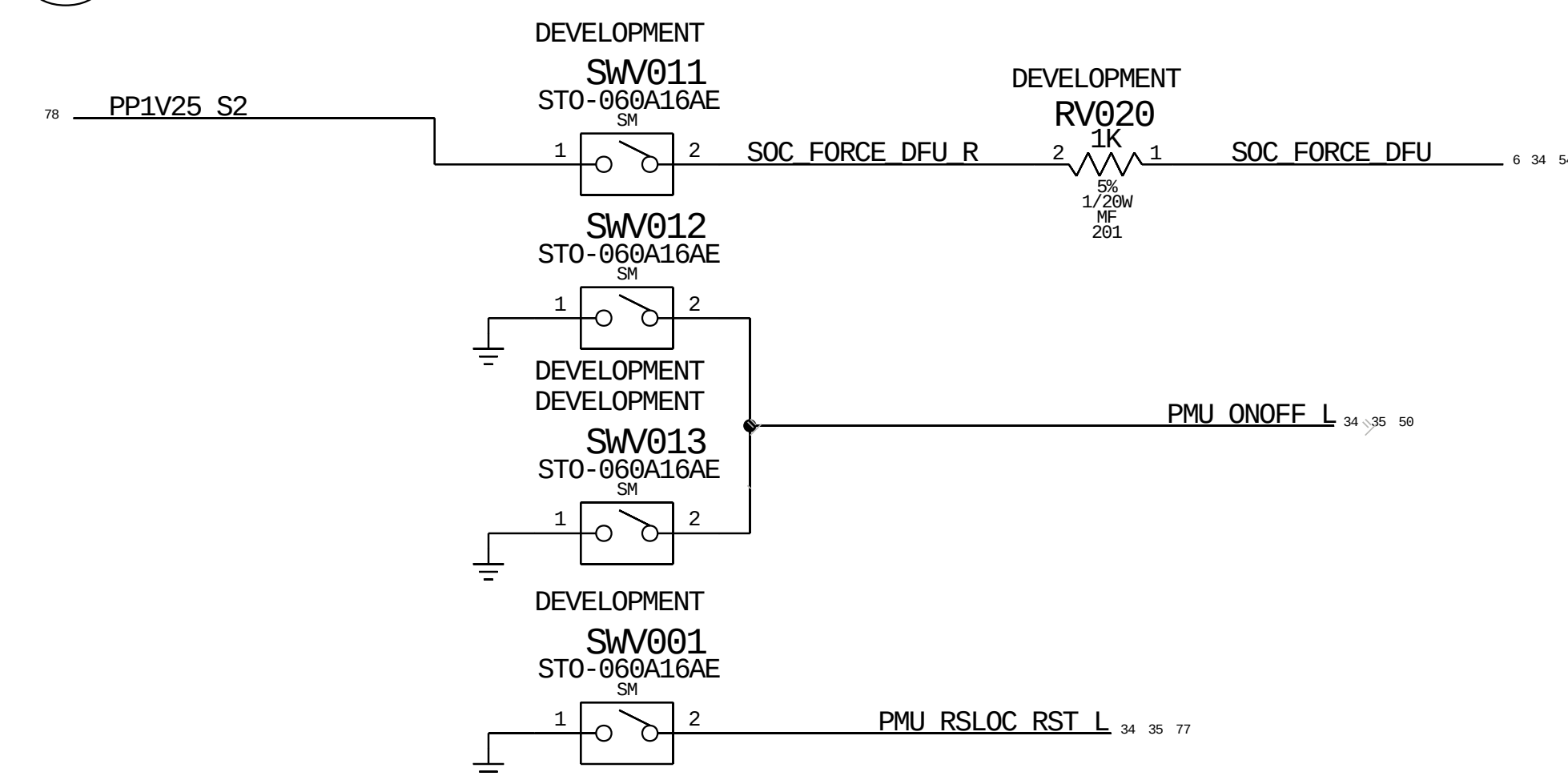
	TPT_P3V8A0N_PU_RAIL	==	MAKE_BASE=TRUE	TPT_P3V8A0N_PU_RAIL	25
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6	NC_FPWM2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_FPWM2
6	NC_SWD_TMS3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS3
6	NC_SWD_TMS4	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS4
7	NC_I2S3_BCLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_BCLK
7	NC_I2S3_D2R	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_D2R
7	NC_I2S3_LRCLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_LRCLK
7	NC_I2S3_MCLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_MCLK
7	NC_I2S3_R2D	==	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_R2D
7	NC_SOC_GPIO01	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO01
7	IPD_SPT_EN	==	MAKE_BASE=TRUE	NO_TEST=1	IPD_SPT_EN
7	NC_SOC_GPIO09	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO09
7	NC_SOC_GPIO10	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO10
7	NC_SOC_GPIO15	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO15
7	NC_SOC_GPIO16	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO16
7	NC_SOC_I2S0_MCK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S0_MCK
7	NC_SOC_I2S1_MCK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S1_MCK
7	NC_SOC_I2S2_MCK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S2_MCK
7	NC_SOC_SPI2_SSIN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_SPI2_SSIN
7	NC_SPMI2_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_CLK
7	NC_SPMI2_DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_DATA
7	NC_SSP10_MOSI	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SSP10_MOSI
7	NC_UART3_D2R	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R
7	NC_UART3_D2R_CTS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R_CTS_L
7	NC_UART3_R2D	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D
7	NC_UART3_R2D_RTS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D_RTS_L
7	NC_UART4_D2R	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R
7	NC_UART4_D2R_CTS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R_CTS_L
7	NC_UART4_R2D	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D
7	NC_UART4_R2D_RTS_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D_RTS_L
7	NC_UART7_RXD	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_RXD
7	NC_UART7_TXD	==	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_TXD
8	NC_DISP_FSYNC	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_FSYNC
8	NC_DISP_SPMI_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_CLK
8	NC_DISP_SPMI_DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_DATA
8	NC_DISP_TOUCH_BSYNC0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC0
8	NC_DISP_TOUCH_BSYNC1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC1
8	NC_DISP_TOUCH_EB	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_EB
8	NC_DISPLAY_POL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_DISPLAY_POL
8	NC_ISP_GPIO1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO1
8	NC_ISP_GPIO2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO2
8	NC_ISP_GPIO3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO3
8	NC_ISP_I2C0_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SCL
8	NC_ISP_I2C0_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SDA
8	NC_ISP_I2C1_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SCL
8	NC_ISP_I2C1_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SDA
8	NC_ISP_I2C3_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SCL
8	NC_ISP_I2C3_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SDA
8	NC_ISP_SPMI0_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_CLK
8	NC_ISP_SPMI0_DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_DATA
8	NC_ISP_SPMI1_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_CLK
8	NC_ISP_SPMI1_DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_DATA
8	NC_LPDP_TX4N	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4N
8	NC_LPDP_TX4P	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4P
8	NC_LPDP_TX5N	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5N
8	NC_LPDP_TX5P	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5P
8	NC_LPDPRX_AUX0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX0
8	NC_LPDPRX_AUX1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX1
8	NC_LPDPRX_AUX2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX2
8	NC_LPDPRX_AUX3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX3
8	NC_LPDPRX_AUX4	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX4
8	NC_LPDPRX_AUX5	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX5
8	NC_LPDPRX_AUX6	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX6
8	NC_LPDPRX_AUX7	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX7
8	NC_LPDPRX_AUX8	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX8
8	NC_LPDPRX_AUX9	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX9
8	NC_LPDPRX_AUX10	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX10
8	NC_LPDPRX_AUX11	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX11
8	NC_MIPI0C_CLKN	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKN
8	NC_MIPI0C_CLKP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKP
8	NC_MIPI0C_DATAN0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN0
8	NC_MIPI0C_DATAN1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN1
8	NC_MIPI0C_DATAP0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP0
8	NC_MIPI0C_DATAP1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP1
8	NC_SENSOR0_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR0_CLK
8	NC_SENSOR1_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR1_CLK
8	NC_SENSOR2_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR2_CLK
8	NC_SENSOR3_CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR3_CLK
9	NC_NAND0_PCIE_RESET1_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_PCIE_RESET1_L
9	NC_PAD_MTR_ANALOG_TEST_NEG	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_NEG
9	NC_PAD_MTR_ANALOG_TEST_POS	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_POS
9	NC_PAD_MTR_VREF_NEG	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_NEG
9	NC_PAD_MTR_VREF_POS	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_POS
10	NC_AON_SLEEP1_RESET_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AON_SLEEP1_RESET_L
10	NC_AOP_FUNC1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC1
10	NC_AOP_FUNC5	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC5
10	NC_AOP_FUNC10	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC10
10	NC_AOP_FUNC14	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC14
10	NC_AOP_SPMI0_SCLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SCLK
10	NC_AOP_SPMI0_SDATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SDATA
10	NC_AOP_UART2_D2R	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_D2R
10	NC_AOP_UART2_R2D	==	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_R2D

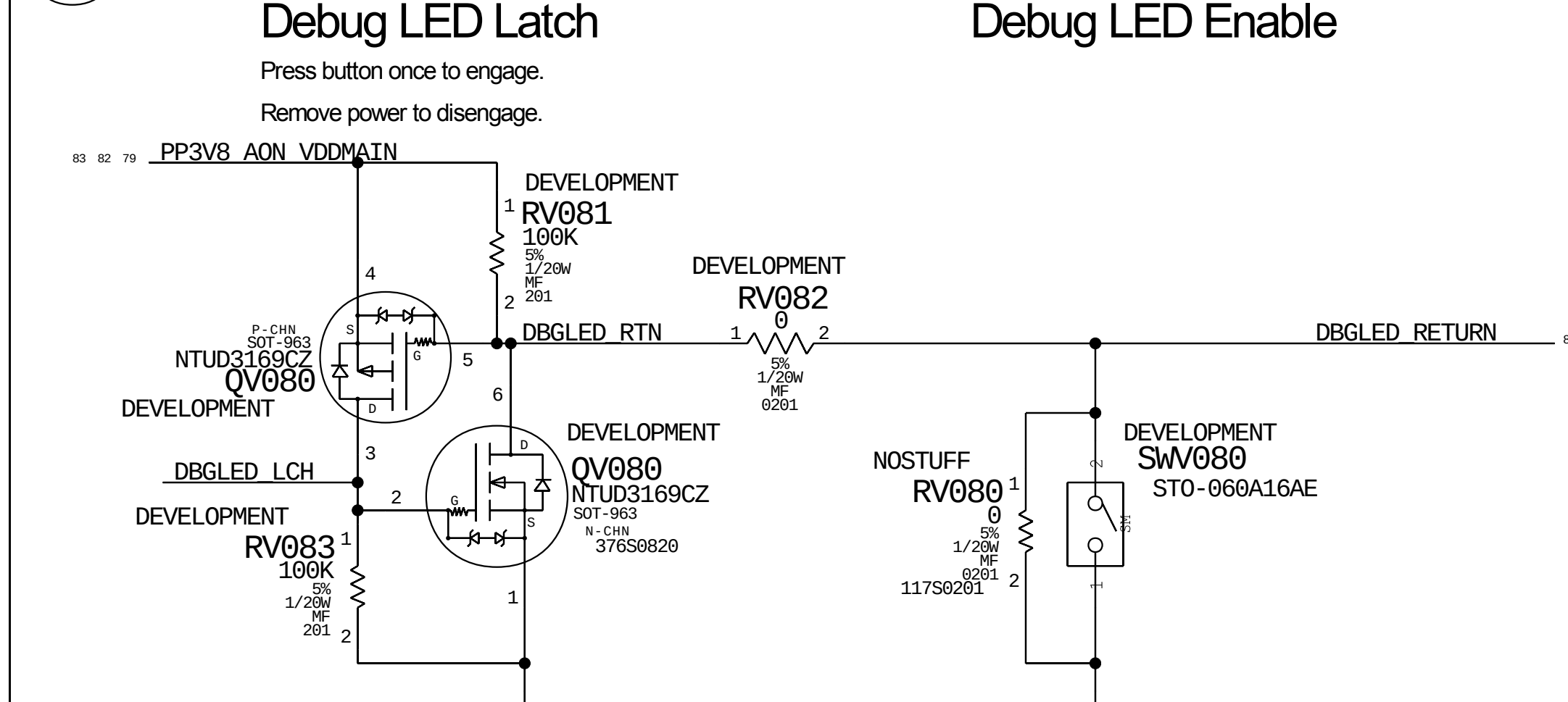
10	NC_PDM_CLK1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK1
10	NC_PDM_CLK2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK2
10	NC_PDM_CLK5	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK5
10	NC_PDM_CLK6	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK6
10	NC_PDM_DATA1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA1
10	NC_PDM_DATA2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA2
10	NC_SMC_GPIO1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GPIO1

23	NC_CHGR_CBC_ON	==	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_CBC_ON
23	NC_CHGR_EN_VR1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_EN_VR1
23	NC_CHGR_SMC_RST_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_SMC_RST_L
58	NC_EUSB_LS1N	==	MAKE_BASE=TRUE	NO_TEST=1	NC_EUSB_LS1N
58	NC_EUSB_LS1P	==	MAKE_BASE=TRUE	NO_TEST=1	NC_EUSB_LS1P
21	NC_SE_GP100	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SE_GP100
51	NC_SMBUS_ATCR1MR0_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCR1MR0_SCL
51	NC_SMBUS_ATCR1MR0_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCR1MR0_SDA
52	NC_SMBUS_ATCR1MR1_SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCR1MR1_SCL
52	NC_SMBUS_ATCR1MR1_SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCR1MR1_SDA
58	NC_USB_LS1N	==	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1N
58	NC_USB_LS1P	==	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1P
8	NC_LPDPRX_RXN0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN0
8	NC_LPDPRX_RXN1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN1
8	NC_LPDPRX_RXN2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN2
8	NC_LPDPRX_RXN3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN3
8	NC_LPDPRX_RXN4	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN4
8	NC_LPDPRX_RXN5	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN5
8	NC_LPDPRX_RXN6	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN6
8	NC_LPDPRX_RXN7	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN7
8	NC_LPDPRX_RXN8	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN8
8	NC_LPDPRX_RXN9	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN9
8	NC_LPDPRX_RXN10	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN10
8	NC_LPDPRX_RXN11	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN11
8	NC_LPDPRX_RXP0	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP0
8	NC_LPDPRX_RXP1	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP1
8	NC_LPDPRX_RXP2	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP2
8	NC_LPDPRX_RXP3	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP3
8	NC_LPDPRX_RXP4	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP4
8	NC_LPDPRX_RXP5	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP5
8	NC_LPDPRX_RXP6	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP6
8	NC_LPDPRX_RXP7	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP7
8	NC_LPDPRX_RXP8	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP8
8	NC_LPDPRX_RXP9	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP9
8	NC_LPDPRX_RXP10	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP10
8	NC_LPDPRX_RXP11	==	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP11
62	NC_NAND0_S5E0_VPP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E0_VPP
63	NC_NAND0_S5E1_VPP	==	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E1_VPP

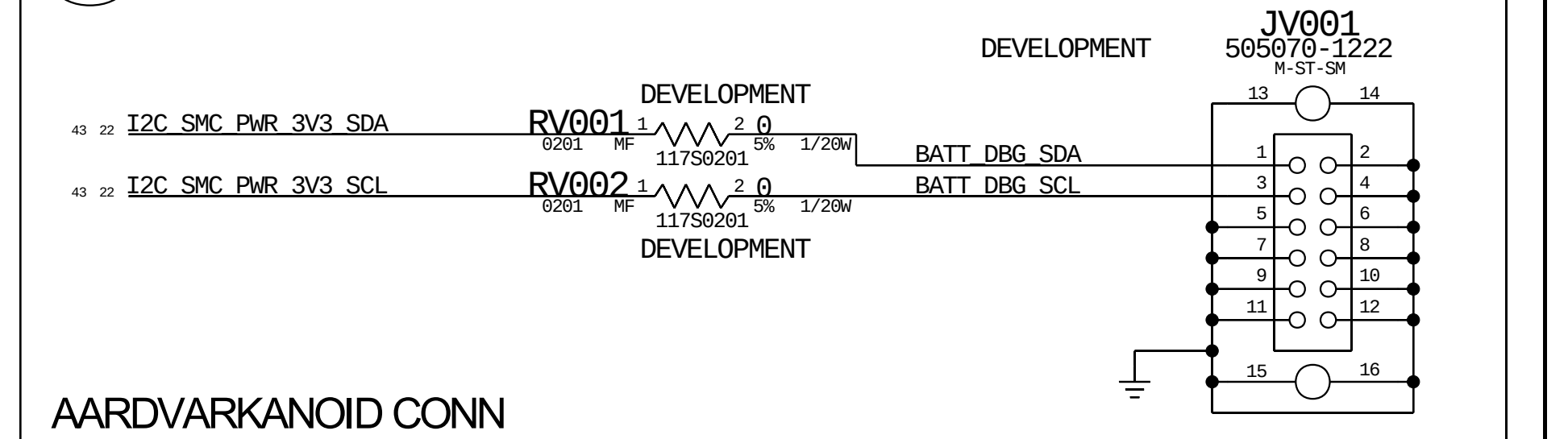
A Debug Push-Buttons



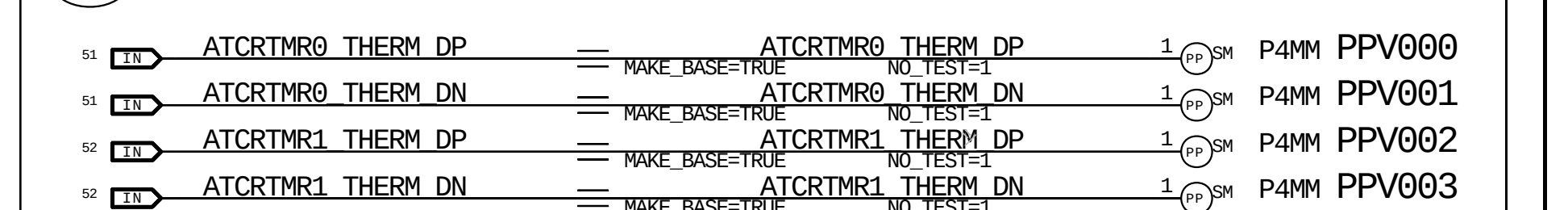
B Debug LED Control



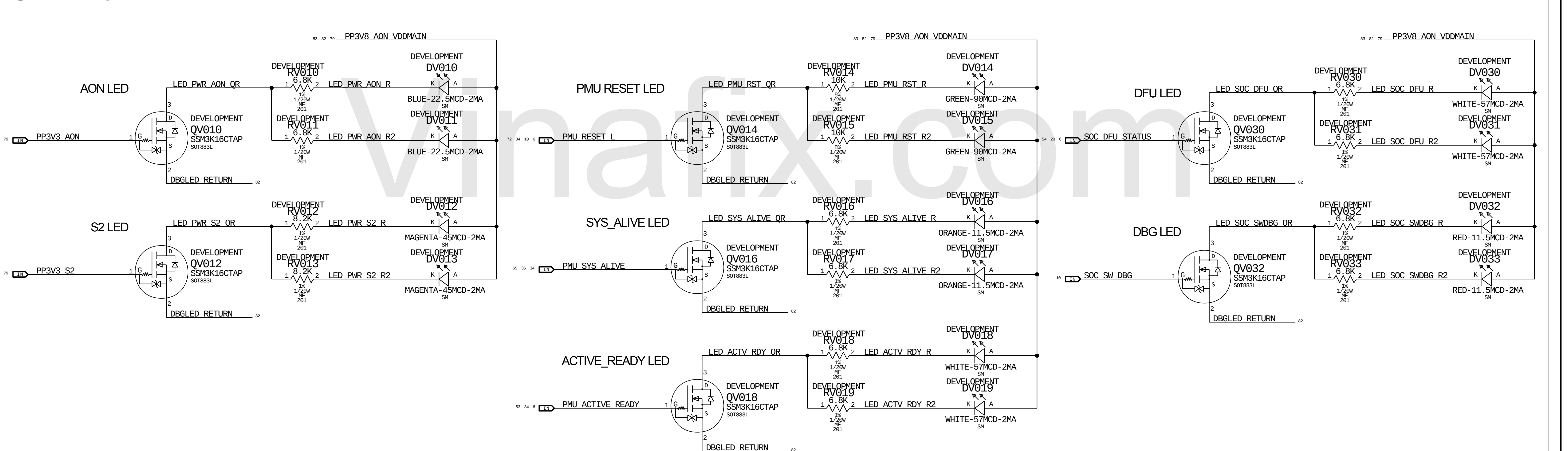
C Battery Sub-System Debug Connector



D Thermal Diode Test Points



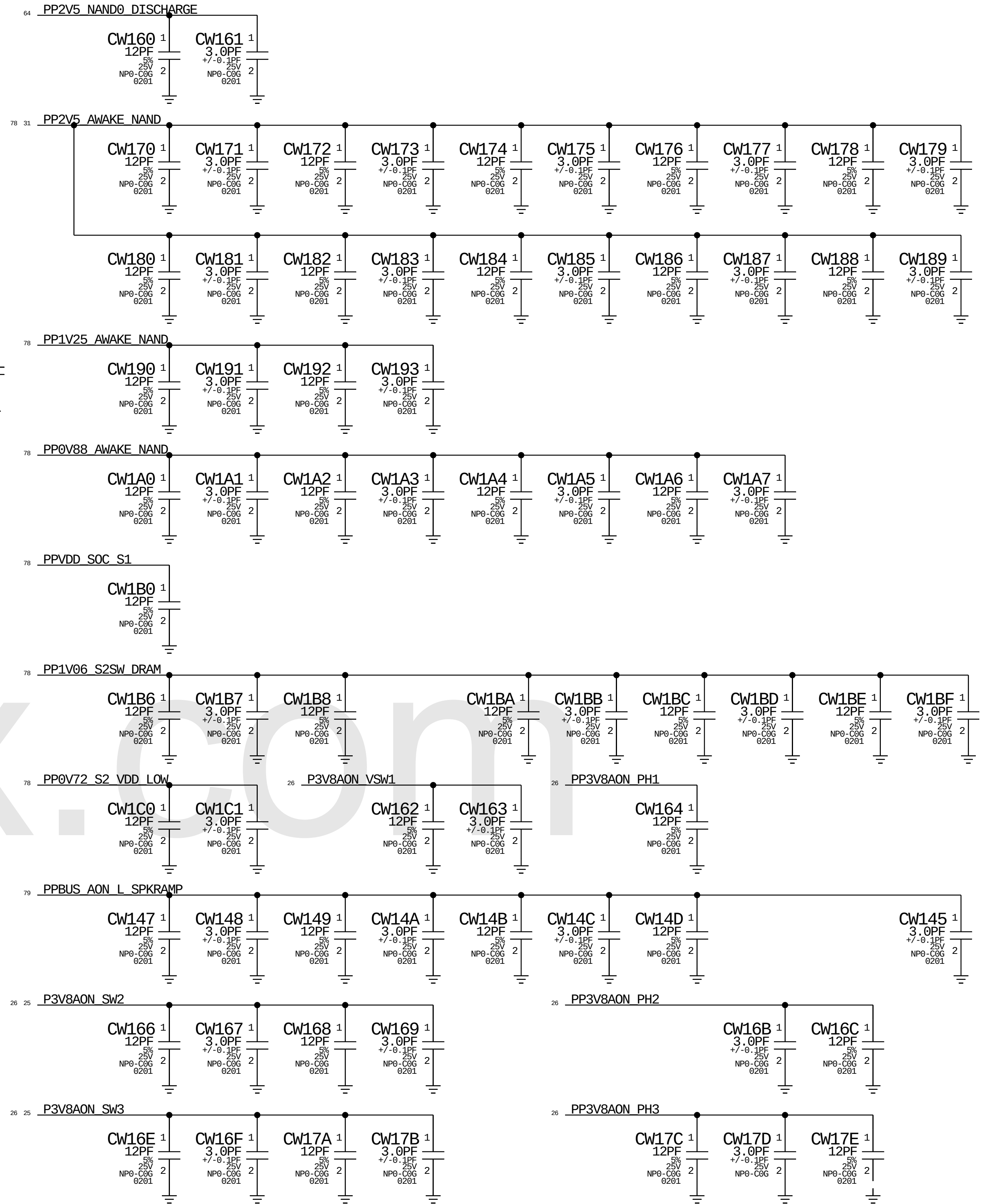
E Debug LEDs



8



4



BOM_COST_GROUP=DESENSE

Desense

SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS		COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*		CLASS STATUS
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SMD	P	A_45_OHM_SE	SMD_NAND*,SMD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL*,*JTAG*TCK*,*JTAG*TDI*,*JTAG*TD0*,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O_R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
CIO_D2R	P	A_85_OHM_DIFF	DP:DP_USBC*_D2R*	Y
CIO_R2D	P	A_85_OHM_DIFF	DP:DP_USBC*_R2D*	Y
PCIE_NAND_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_D2R*	Y
PCIE_NAND_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_R2D*	Y
PCIE_WLBT_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_R2D*	Y
PCIE_WLBT_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP:DP_LPDP_INT_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M*	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
MIPI_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_CLK*,DP_MIPI_CLOCK*	Y
MIPI_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_DATA*,DP_MIPI_DATA*	Y
EUSB	P	A_85_OHM_DIFF	DP:DP_EUSB*	Y
GROUND	P	DEFAULT	GND	Y
POWER	P	POWER	PP*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

NET NAME	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS NUMBER
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:.)	Y/N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_9X	=	Y
CIO_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_WLBT_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WLBT_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_CLK	S	A_DIELECTRIC_6X	=	Y
LPDP	S	A_DIELECTRIC_6X	=	Y
MIPI_CLK	S	A_DIELECTRIC_5X	=	Y
MIPI_DATA	S	A_DIELECTRIC_5X	=	Y
EUSB	S	A_DIELECTRIC_5X	=	Y
GROUND	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y
RF	S	RF	RF_ANT*	Y

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	MIPI_CLK	A_DIELECTRIC_4X
CIO_D2R	MIPI_DATA	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_CLK	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_CLK	A_DIELECTRIC_4X
MIPI_DATA	MIPI_CLK	A_DIELECTRIC_2X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08813	1	PCBA,KANHA,X1711	U0600	CRITICAL	CPU:INTERPOSER

A1 BEST

998-21412	1	SOC,TGA A1+86,1Y,8C,DEV,CX,H,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_BEST
998-21413	998-21412	CPU:SOC_A1_HYNIX_8GB_BEST	ALL	SCK	
998-21414	1	SOC,TGA A1+86,1Y,8C,DEV,CX,M,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_BEST
998-21415	998-21414	CPU:SOC_A1_MICRON_8GB_BEST	ALL	SCK	
998-21416	1	SOC,TGA A1+166,1Y,8C,DEV,CX,H,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_BEST
998-21417	998-21416	CPU:SOC_A1_HYNIX_16GB_BEST	ALL	SCK	
998-21418	1	SOC,TGA A1+166,1X,8C,DEV,CX,M,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_BEST
998-21420	998-21418	CPU:SOC_A1_MICRON_16GB_BEST	ALL	SCK	

A1 GOOD

998-21421	1	SOC,TGA A1+86,1Y,7C,DEV,CX,H,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_GOOD
998-21422	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK	
998-21412	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	ACK	
998-21413	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK	
998-21423	1	SOC,TGA A1+86,1Y,7C,DEV,CX,M,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_GOOD
998-21424	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK	
998-21414	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	ACK	
998-21415	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK	
998-21426	1	SOC,TGA A1+166,1Y,7C,DEV,CX,H,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_GOOD
998-21427	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK	
998-21416	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	ACK	
998-21417	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK	
998-21428	1	SOC,TGA A1+166,1X,7C,DEV,CX,M,ATK,M02562	U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_GOOD
998-21429	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK	
998-21418	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	ACK	
998-21420	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK	

B0 BEST

998-22388	1	SOC,TGA B0+86,1Y,8C,LP,DEV,CX,H,A,M02562	U0600	CRITICAL	CPU:SOC_HYNIX_8GB_BEST
998-22387	998-22388	CPU:SOC_HYNIX_8GB_BEST	ALL	SCK	
998-22386	1	SOC,TGA B0+86,1Y,8C,LP,DEV,CX,M,A,M02562	U0600	CRITICAL	CPU:SOC_MICRON_8GB_BEST
998-22385	998-22386	CPU:SOC_MICRON_8GB_BEST	ALL	SCK	
998-22392	1	SOC,TGA B0+166,1Y,8C,LP,DEV,CX,H,A,M02562	U0600	CRITICAL	CPU:SOC_HYNIX_16GB_BEST
998-22391	998-22392	CPU:SOC_HYNIX_16GB_BEST	ALL	SCK	
998-22390	1	SOC,TGA B0+166,1X,8C,LP,DEV,CX,M,A,M02562	U0600	CRITICAL	CPU:SOC_MICRON_16GB_BEST
998-22389	998-22390	CPU:SOC_MICRON_16GB_BEST	ALL	SCK	

B0 GOOD

998-22404	1	SOC,TGA B0+86,1Y,7C,LP,DEV,CX,H,A,M02562	U0600	CRITICAL	CPU:SOC_HYNIX_8GB_GOOD
998-22403	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK	
998-22388	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	ACK	
998-22387	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK	
998-22402	1	SOC,TGA B0+86,1Y,7C,LP,DEV,CX,M,A,M02562	U0600	CRITICAL	CPU:SOC_MICRON_8GB_GOOD
998-22401	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK	
998-22386	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	ACK	
998-22385	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK	
998-22409	1	SOC,TGA B0+166,1Y,7C,LP,DEV,CX,H,A,M02562	U0600	CRITICAL	CPU:SOC_HYNIX_16GB_GOOD
998-22408	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK	
998-22392	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	ACK	
998-22391	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK	
998-22407	1	SOC,TGA B0+166,1X,7C,LP,DEV,CX,M,A,M02562	U0600	CRITICAL	CPU:SOC_MICRON_16GB_GOOD
998-22406	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK	
998-22390	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	ACK	
998-22389	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK	

NAND Landing 0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND_L0:SSE_STUDY
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,2566,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_TO
335S00470	1	NAND,3DV4,128GBT,XXX,SSE,2566,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_SD
335S00437	1	NAND,3DV5,128GB,SSE,5126,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_HY
335S00489	1	NAND,3DV4,160GBT,XXX,SSE,2566,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_SD
335S00480	1	NAND,3DV4,160GBT,XXX,SSE,2566,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_TO
335S00482	1	NAND,3DV5,320GB,SSE,5126,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_HY
335S00481	1	NAND,3DV4,280GBT,XXX,SSE,2566,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,SSE,2566,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,2566,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TB0T,XXX,SSE,5126,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1624GBT,SSE,5126,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND_L0:INTERPOSER

NAND Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND_L1:SSE_STUDY
335S00437	1	NAND,3DV5,128GB,SSE,5126,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_HY
335S00470	1	NAND,3DV4,128GBT,XXX,SSE,2566,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_SD
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,2566,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_TO
335S00438	1	NAND,3DV5,256GB,SSE,5126,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_HY
335S00464	1	NAND,3DV4,256GBT,XXX,SSE,2566,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,SSE,2566,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,2566,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TB0T,XXX,SSE,5126,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1624GBT,SSE,5126,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND_L1:INTERPOSER

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20066	1	IC,PMU,SPMU,A0,OTP-JPC,MLCSP196	U7700	CRITICAL	SPMU_IC:DEV
998-22526	1	IC,PMU,SIMETRA,A1,OTP-JPE,MLCSP196	U7700	CRITICAL	SPMU_IC:A1

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20064	1	IC,PMU,MPMU,A0,OTP-JPE,MLCSP440	U8100	CRITICAL	MPMU_IC:DEV
998-22614	1	IC,PMU,SERA,B0,OTP-JPF,MLCSP440	U8100	CRITICAL	MPMU_IC:B0

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG:ITLC_S5E_128G_TO	NAND_L0:ITLC_128G_TO
NANDCFG:ITLC_S5E_128G_SD	NAND_L0:ITLC_128G_SD
NANDCFG:ITLC_S5E_256G_HY	NAND_L0:ITLC_256G_HY,NAND_L1:ITLC_256G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_SD	NAND_L0:ITLC_256G_SD,NAND_L1:ITLC_256G_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_TO	NAND_L0:ITLC_256G_TO,NAND_L1:ITLC_256G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_HY	NAND_L0:ITLC_512G_HY,NAND_L1:ITLC_512G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_TO	NAND_L0:ITLC_512G_TO,NAND_L1:ITLC_512G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_SD	NAND_L0:ITLC_1P0T_SD,NAND_L1:ITLC_1P0T_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_TO	NAND_L0:ITLC_1P0T_TO,NAND_L1:ITLC_1P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_TO	NAND_L0:ITLC_2P0T_TO,NAND_L1:ITLC_2P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_HY	NAND_L0:ITLC_2P0T_HY,NAND_L1:ITLC_2P0T_HY,PARTS_SSDNAND1
NANDCFG:INTERPOSER	NAND_L0:INTERPOSER,NAND_L1:INTERPOSER,PARTS_SSDNAND1
NANDCFG:NONE	NAND_L0:OFF,NAND_L1:OFF,PARTS_SSDNAND1

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Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS :
353S01346	353S01320		ALL	rdar:///problem/57736570
138S0738	138S1101		ALL	rdar:///problem/59471481
138S0846	138S0811		ALL	rdar:///problem/59474499
376S1053	376S0604		ALL	rdar:///problem/59475163
152S00359	152S00253		ALL	rdar:///problem/57204466
740S06041	740S0159		ALL	rdar:///problem/59438987
371S00077	371S00180		ALL	rdar:///problem/59475330
376S1106	376S0678		ALL	rdar:///problem/59442581
107S00033	107S00034		ALL	rdar:///problem/59471987
138S00087	138S1086		ALL	rdar:///problem/59438865
152S00812	152S1701		ALL	rdar:///problem/59465659
371S00217	371S00079		ALL	rdar:///problem/57730774
376S0948	376S00076		ALL	rdar:///problem/59134310
128S00031	128S00011		ALL	rdar:///problem/59071370
128S00026	128S00011		ALL	rdar:///problem/59071370
128S00087	128S00011		ALL	rdar:///problem/59071370
128S0445	128S0436		ALL	rdar:///problem/59071568
128S0364	128S0264		ALL	rdar:///problem/59071705
128S00094	128S00067		ALL	rdar:///problem/59072397
128S00039	128S00038		ALL	rdar:///problem/59075402
128S0302	128S00038		ALL	rdar:///problem/59075402
152S00600	152S00198		ALL	rdar:///problem/59075547
152S00383	152S00198		ALL	rdar:///problem/59075547
152S00708	152S00265		ALL	rdar:///problem/59075783
152S00367	152S01248		ALL	rdar:///problem/59076041
376S00204	376S00203		ALL	rdar:///problem/59076791
376S00226	376S00203		ALL	rdar:///problem/59076791
376S00227	376S00203		ALL	rdar:///problem/59076791
376S00228	376S1179		ALL	rdar:///problem/59077240
376S00007	376S1179		ALL	rdar:///problem/59077240
376S00303	376S00012		ALL	rdar:///problem/59077463
376S1147	376S00281		ALL	rdar:///problem/59077604
107S00071	107S00053		ALL	rdar:///problem/59078523
107S00029	107S00007		ALL	rdar:///problem/59081345
138S00332	138S00328		ALL	rdar:///problem/59112527
138S00047	138S00073		ALL	rdar:///problem/59118124
138S0063	138S0053		ALL	rdar:///problem/59118514
138S00077	138S00035		ALL	rdar:///problem/59119189
138S00093	138S00035		ALL	rdar:///problem/59119189
138S00116	138S00071		ALL	rdar:///problem/59119528
138S00117	138S00071		ALL	rdar:///problem/59119528
138S00229	138S00107		ALL	rdar:///problem/59123509
138S00022	138S0001		ALL	rdar:///problem/59124126
152S00398	152S00204		ALL	rdar:///problem/59129606
152S00063	152S00085		ALL	rdar:///problem/59129928
152S00343	152S000839		ALL	rdar:///problem/59130255
152S01317	152S01268		ALL	rdar:///problem/59130415
152S00997	152S00476		ALL	rdar:///problem/59130875
152S01090	152S01085		ALL	rdar:///problem/59131117
107S00055	107S00090		ALL	rdar:///problem/59082308
107S00365	107S000373		ALL	rdar:///problem/59081538
152S01344	152S00883		ALL	rdar:///problem/59353109
152S00979	152S00074		ALL	rdar:///problem/59364196
197S00046	197S00036		ALL	rdar:///problem/59408673
197S00047	197S00036		ALL	rdar:///problem/59408673
197S00048	197S00036		ALL	rdar:///problem/59408673
138S00101	138S0035		ALL	rdar:///problem/59408752
138S00291	138S0035		ALL	rdar:///problem/59408752
377S00166	377S00160		ALL	rdar:///problem/59407974
138S00330	138S00001		ALL	rdar:///problem/59408011
740S0118	740S00028		ALL	rdar:///problem/59400586
377S00123	377S00031		ALL	rdar:///problem/59407768
377S00106	377S00000		ALL	rdar:///problem/59407847

Alternate Vendor	Primary Vendor
On Semi	NXP
Samsung	Murata
Samsung	Murata
Diodes Inc	On Semi
Chilisin	Cyntec
Bourns	LittleFuse
NXP	Diodes Inc
On Semi	Vishay
TFT	Cyntec
Taiyo Yuden	Murata
Chilisin	Cyntec
ROHM CORP	Nexperia
Diodes Inc	Toshiba
ROHM CORP	Kemet
NEC/Kemet	Kemet
Panasonic	Kemet
Panasonic	Kemet
Kemet	Panasonic
Tokin/Kemet	Panasonic
NEC/Kemet	Kemet
Panasonic	Kemet
Chilisin	Cyntec
Vishay	Cyntec
Chilisin	Cyntec
NEC	Cyntec
Diodes Inc	Vishay
Vishay	Vishay
Fairchild	Vishay
On Semi	Vishay
AOS	Vishay
Diodes Inc	TI
On Semi	AOS
Yageo	Cyntec
TFT	Yageo
Kyocera	Murata
Taiyo	Murata
Taiyo	Murata
Taiyo	Murata
Kyocera	Murata
Kyocera	Murata
Taiyo	Murata
Taiyo	Cyntec
Taiyo	Cyntec
Murata	Cyntec
Taiyo	Cyntec
Chilisin	Murata
Chilisin	Murata
Cyntec	TFT
Cyntec	TFT
Chilisin	Cyntec
Taiyo	Cyntec
Epson	TXC
Kyocera	TXC
Murata	TXC
Samsung	Murata
Kyocera	Murata
Semtech	On Semi
SEMCO	Murata
Polytronics	Bussmann
Semtech	On Semi
Semtech	ST Micro

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS :
371S00220	371S00181		ALL	rdar:///problem/59404055
371S00085	371S00190		ALL	rdar:///problem/59404093
353S00852	353S4262		ALL	rdar:///problem/59403423
311S00156	311S00129		ALL	rdar:///problem/59409000
376S1080	376S0820		ALL	rdar:///problem/59409026
138S00049	138S0831		ALL	rdar:///problem/59406790
311S00269	311S00234		ALL	rdar:///problem/59409341
311S00176	311S00153		ALL	rdar:///problem/59409111
311S00178	311S00177		ALL	rdar:///problem/59409119
376S1128	376S00282		ALL	rdar:///problem/59409044
376S00224	376S00282		ALL	rdar:///problem/59409044
128S00093	128S00009		ALL	rdar:///problem/59125761
128S00103	128S00009		ALL	rdar:///problem/59125761
128S00106	128S00009		ALL	rdar:///problem/59361958
128S00107	128S00009		ALL	rdar:///problem/59361958
128S00110	128S00009		ALL	rdar:///problem/59361958
376S1137	376S00019		ALL	rdar:///problem/59409062
107S00101	107S00005		ALL	TBD
107S00102	107S00017		ALL	TBD
107S0276	107S00020		ALL	TBD
107S00370	107S00371		ALL	TBD
107S00372	107S00371		ALL	TBD
107S00298	107S0208		ALL	TBD
107S0150	107S0208		ALL	TBD
116S00007	116S00006		ALL	TBD
132S0400	132S00064		ALL	TBD
132S0012	132S0401		ALL	TBD
138S00084	138S00060		ALL	TBD
138S00750	138S00097		ALL	TBD
138S00204	138S00136		ALL	TBD
138S0052	138S0018		ALL	TBD
138S0789	138S0041		ALL	TBD
155S0275	155S00108		ALL	TBD
155S0706	155S0302		ALL	TBD
155S0741	155S0361		ALL	TBD
155S0023	155S0044		ALL	TBD
155S00007	155S0067		ALL	TBD
155S00190	155S00914		ALL	TBD
138S0706	138S0739		ALL	rdar:///problem/59571433
311S00267	311S000244		ALL	TBD
311S00268	311S00246		ALL	TBD
311S00060	311S0273		ALL	TBD
311S00013	311S0508		ALL	TBD
353S02402	353S1429		ALL	TBD
353S02440	353S3608		ALL	rdar:///problem/59082314
740S0144	740S00028		ALL	TBD
138S00343	138S00329		ALL	rdar:///problem/00090733
376S00292	376S1140		ALL	rdar:///problem/00200671
740S00001	740S00053		ALL	rdar:///problem/00394183

Alternate Vendor	Primary Vendor
On Semi	Diodes Inc
On Semi	Diodes Inc
On Semi	Diodes Inc
Nexperia	TI
Diodes Inc	On Semi
Kyocera	Murata
Nexperia	TI
Diodes Inc	TI
On Semi	TI
Diodes Inc	On Semi
Nexperia	On Semi
Tokin/Kemet	Kemet
Samsung	Kemet
Tokin/Kemet	Kemet
Kemet	Kemet
Samsung	Kemet
Vishay	Diodes Inc
Yageo	Cyntec
Yageo	Cyntec
Cyntec	TFT
Yageo	Cyntec
Vishay	Cyntec
TDK	Murata
Panasonic	Murata
Vishay	Yageo
Taiyo Yuden	Murata
Murata	Taiyo Yuden
Taiyo Yuden	Murata
Murata	Taiyo Yuden
Kyocera	Murata
Samsung	Murata
Samsung	Murata
Taiyo Yuden	Murata
Taiyo Yuden	Murata
Murata	TDK
TDK and Taiyo	Murata
Taiyo Yuden	Panasonic
Taiyo Yuden	Panasonic
Murata	Samsung
Nexperia	TI
Nexperia	TI
Diodes Inc	Philips
Diodes Inc	NXP
ON Semi	TI
ON Semi	TI
Bussman	LittleFuse
Kyocera	Murata
Nexperia	Diodes Inc.
Bourns	AEMI

